EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

Eye Know How

Signal Integrity Consulting

Services and KnowHow

Company Facts

- **Founder:**
  - Dipl. Ing. (FH) Hermann Ruckerbauer
- **Founded:**
  - March 2009
- **Location:**
  - Itzlinger Strasse 21a,
    94469 Deggendorf (Bavaria), Germany
- **Network partners in:**
  - Munich (Design, Layout, CAD)
  - Straubing (EMV)
  - Deggendorf (Lab)
  - China (Shandong und Shaanxi): Oulong Consulting

Hermann Ruckerbauer
Background

- Study of Micro System Technology at University of Applied Sciences in Regensburg
  - Dipl. Ing. (FH) Micro System Technology
- 15 Years experience in Memory Development and High Speed Signaling
  - Siemens: Bench and Production test
  - Infineon / Qimonda:
    - High Speed Signaling
    - Application test
  - Interface standard definition
- Holder of many patents
- EEE Publication:
  - Cascading Techniques for a High-Speed Memory Interface

EKH
Services

- **Consulting for High Speed Signaling**
- **Consulting for Memory Implementation**
- **High speed Simulation and Measurement**
- **Power Delivery Simulation**
- **Model Generation**
- **Measurements**
  - E. g. Logic Analyzer, Scope, TDR, VNA
- **Failure Analysis**
- **PCB Design and Layout**
- **Layout and Design Reviews**
- **Pre-Compliance Measurements on Serial Links**
  - E. g. USB2/3/4, PCIe 2/3/4, SATA; HDMI, …
- **Compliance Measurements on Memory Busses**
  - E. g. DDR2/3/4/5, LPDDR 2/3/4/5, GDDR3/5/6, …

EKH
Cooperation Partners

- **DKH – DesignKnowHow: Dr. Abdallah Bacha**
  - PCB Design and Layout
  - RF Topics
- **SinePulse: Md Sayfullah (www.sinepulse.com)**
  - IT services (India)
  - Hardware development (e. g. FPGA)
- **FH Deggendorf (www.th-deg.de/)**
  - Measurement Lab with VNA and TDR
  - PCB X-section
- **BitIfEye**
  - Measurement Lab for high speed digital signals
- **Rohde&Schwarz**
  - Automated VNA up to 110GHz

EKH
Cooperation Partners

- **EMV – Testhaus (www.emv-testhaus.de)**
  - EMI / EMC compliance test
- **PCB Manufacturing**
  - Ilfa (www.ilfa.de)
  - Elekonta Marek (www.elekonta.de)
- **Assembly**
  - Mair Electronics (www.mair-elektronik.de)
  - Beflex Electronic (www.beflex.de)
- **China Business (Peter Poechmueller)**
  - Oulong Consulting (www.oulongconsulting.com)

Happy Customers

- Bosch
- TQ – Systems
- Kontron
- Congatec
- Micron
- 3D-Plus

Software Tools

- **Keysight ADS (former Agilent)**
  - Time and Frequency domain simulation
  - Analog and Digital Simulation
  - 2.5D and 3D field solver
  - Data evaluation (measurement and simulation)
- **Power Delivery**
  - Cadence Power SI (former Sigrity)
  - Keysight ADS
- **Design and Layout**
  - Cadence Allegro
  - Mentor Hyperlinx/Pads

Software Tools

- **Offline Scope Software**
  - Keysight Infiniium Offline
  - Teledyne MauiStudio
- **S-Parameter post processing**
  - AtaiTec Corp. ADK, x2D, SI3D, and ISD
- **EyeKnowHow internal Software**
  - ADS Data Evaluation: AC/DC Memory Eye Opening
  - DDR Protocol Analysis
  - Cadence to ADS (Layout to Schematic) conversion

Agenda

1) Memory System and Device KnowHow
2) Signal and Power Integrity Simulation
3) Signal and Power Integrity Simulation
4) 2.5D and 3D Modeling for e.g. PCB Layout and Vias
5) Measurement based Modeling
6) Compliance and Correlation Measurement
7) Physical Failure Analysis
8) Design and Layout Services
9) System Optimization
10) EMC / EMI Measurement and Consulting
11) Software and Hardware Products

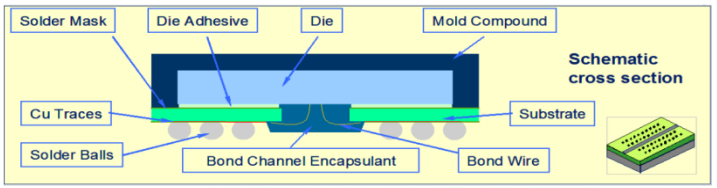
Memory System KnowHow

- **Worked in the development of DDR1 / DDR2 / DDR3 / DDR4**
  - Data and Command/Address bus architecture development
  - Memory Device Specification
- **Consumer, Mobile, Desktop and Server system understanding**
  - Differences in requirements and boundary conditions
- **System requirements**
  - Cache line size limitations
  - Turnaround times, Bandwidth and latency
  - Power limitations
- **Clocking**
  - SSC, Random and Deterministic Jitter
- **Controller functionality**
  - Controller PCI register features (e. g. Delay shift, Driver strength, digital timings)

Memory Device KnowHow

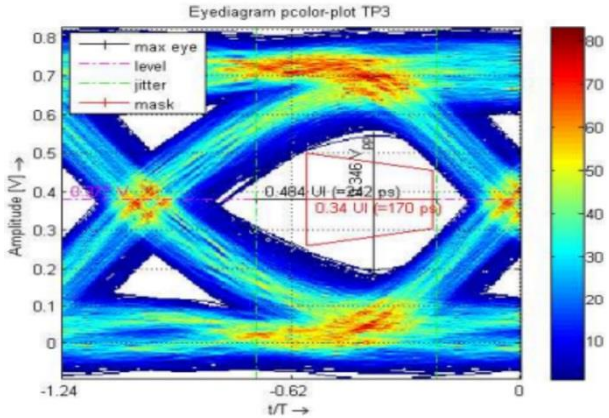
- **Close interaction between System Architecture and DRAM features**
  - IO specification (e. g. Input capacitance, driver and termination linearity)
  - DLL functionality
  - Memory Device Specification
- **DRAM Core / architecture / process limitation**
  - Source for Latency
  - ODOC package and impact on Architecture
  - DRAM process and impact on speed and parasitics
- **DRAM packaging**
  - Planar and stacked DRAM parasitics
  - Wirebond and FCIP packaging

Single Die DRAM Package



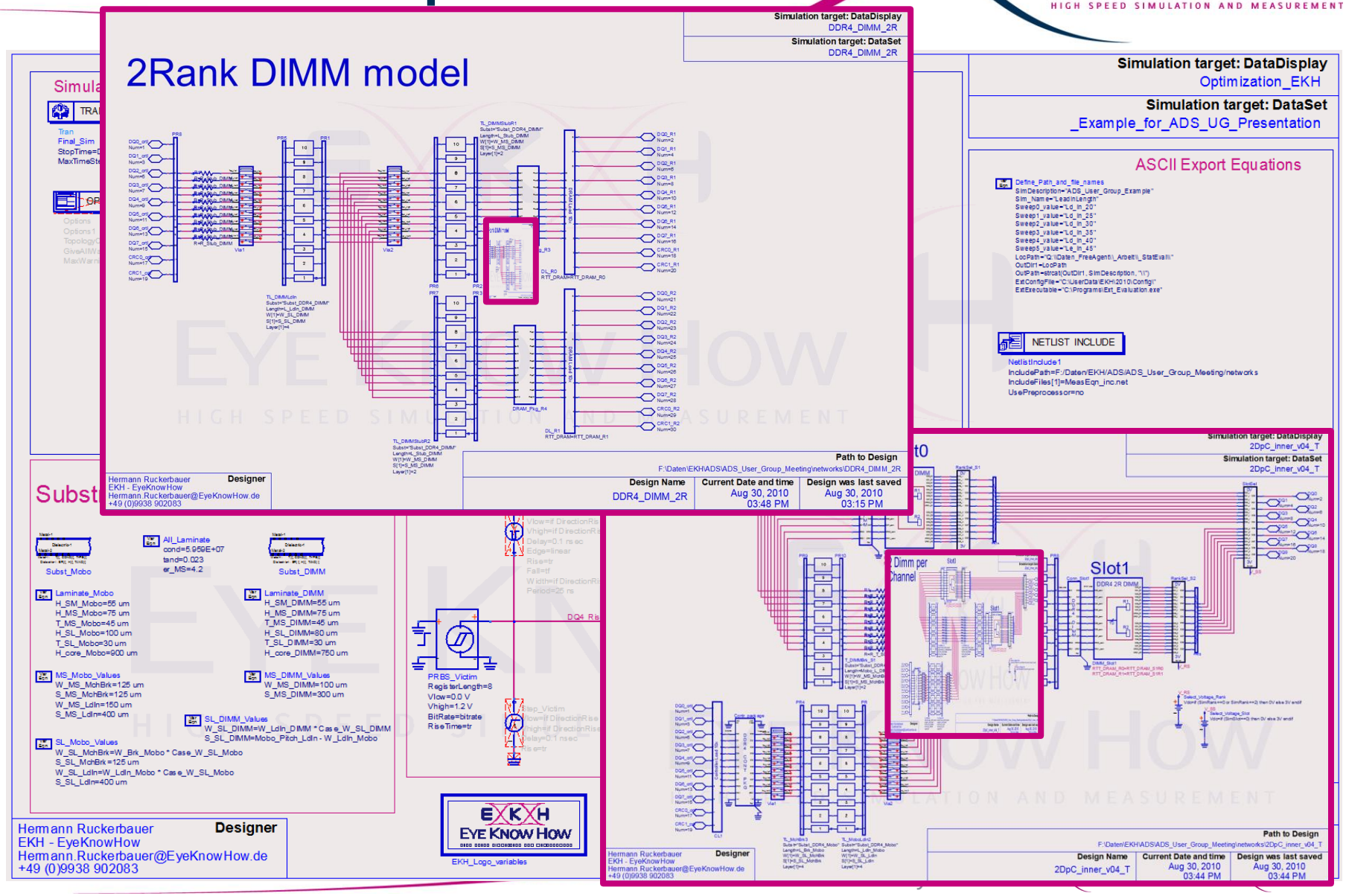
Signal Integrity Simulation

- **Time Domain simulation**
  - Spice models (Lumped elements and BSIM Transistor based)
  - S-Parameter
  - IBIS
- **Frequency Domain simulation**
  - S-Parameter Model Generation
  - Model Comparison
- **Statistical Data Evaluation**
  - Adding Random and Deterministic Jitter
  - Channel Characterization by Step Response
- **Data Eye evaluation**
  - Setup/Hold Evaluation
  - Timing Budget Calculation



Eye Diagram from Channel Step Response

Signal Integrity Simulation Schematic Example



Signal Integrity Simulation Schematic Example

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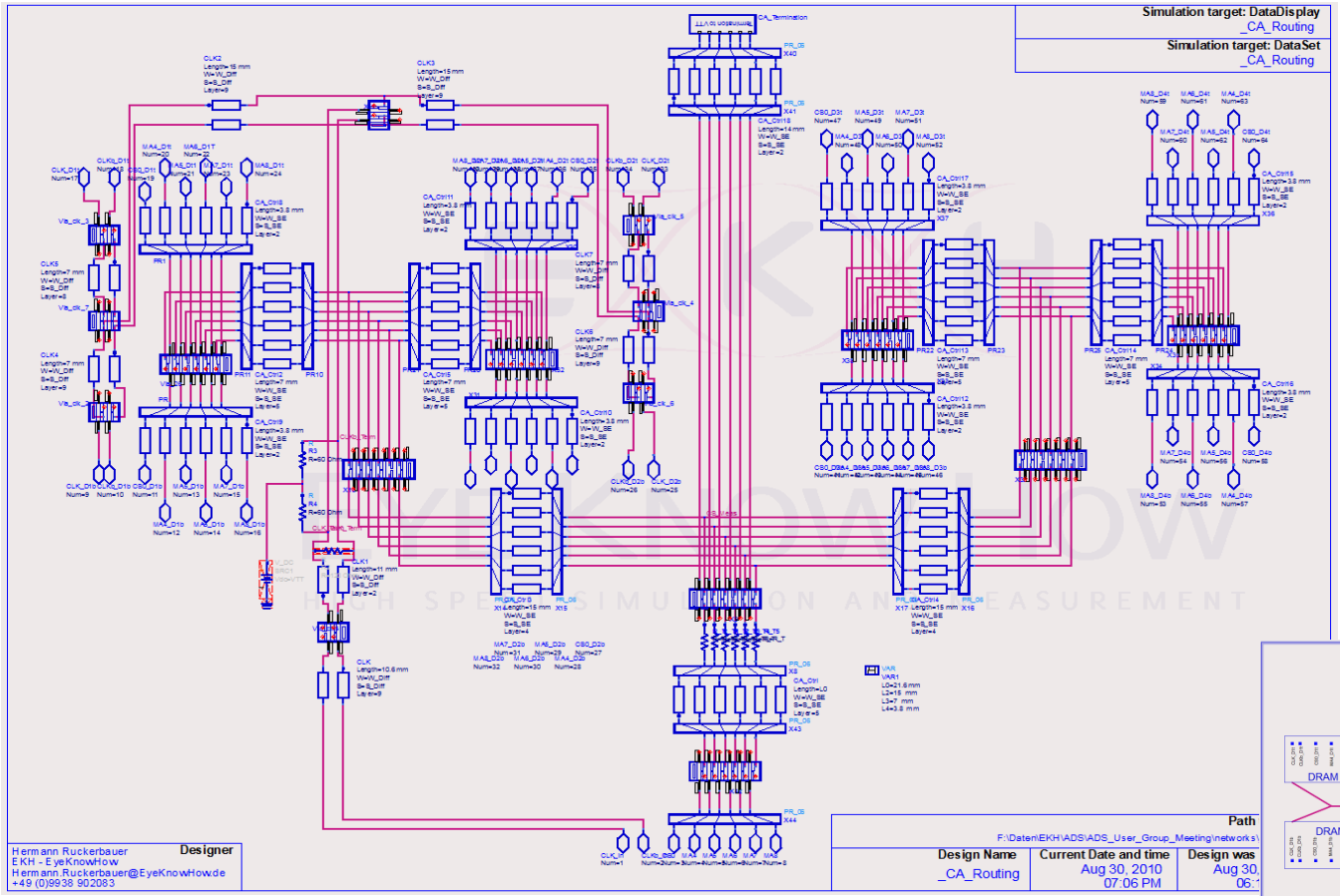
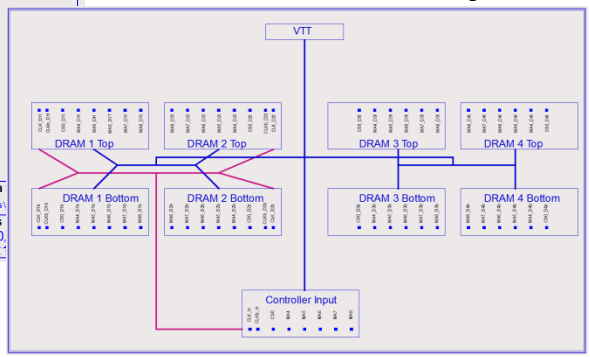
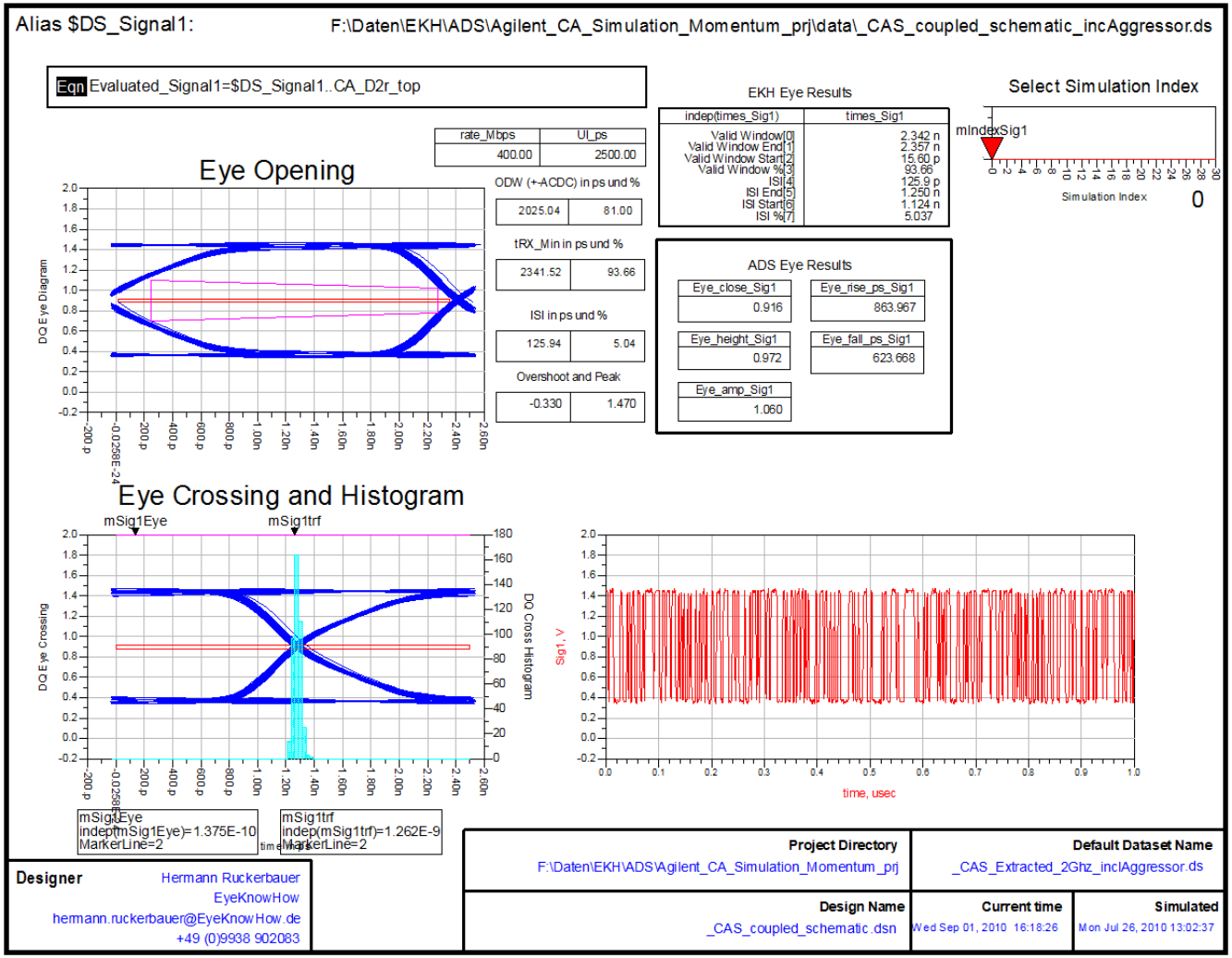


Subcircuit Schematic

Subcircuit Symbol

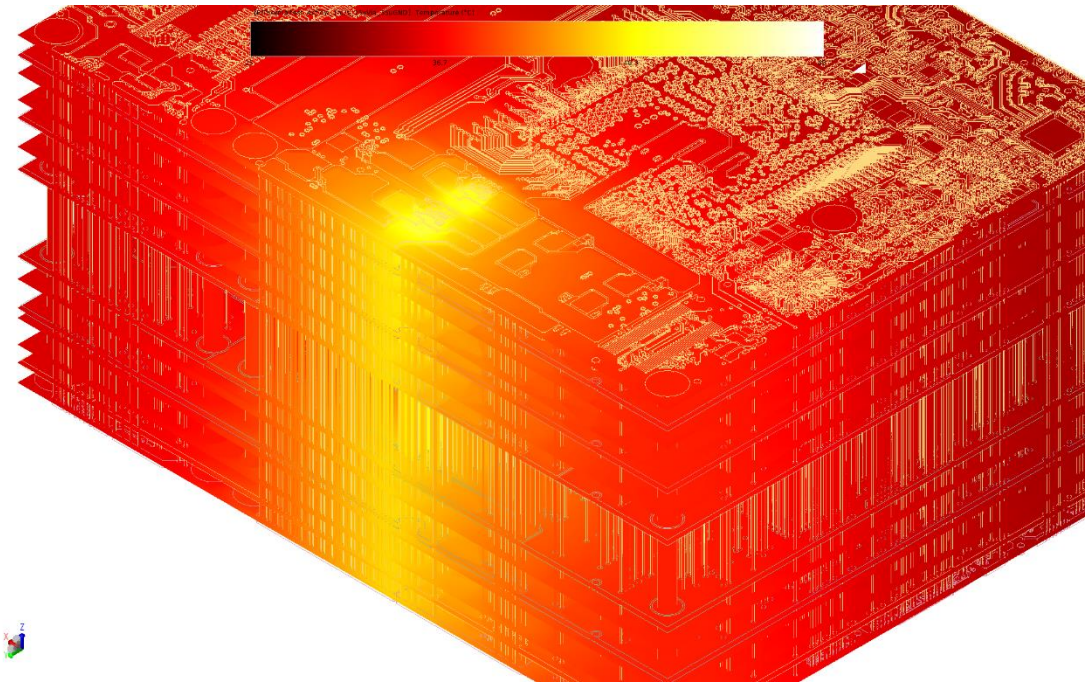


Data Evaluation
DRAM Template Example



Electro-Thermal simulation

- **Electro-Thermal simulation simulation considering thermal impact from devices and PCB copper resistance**



Temperature distribution on a PCB with thermal vias including device power loss and copper resistance power loss.

Power Integrity Simulation
Impedance of Power Delivery

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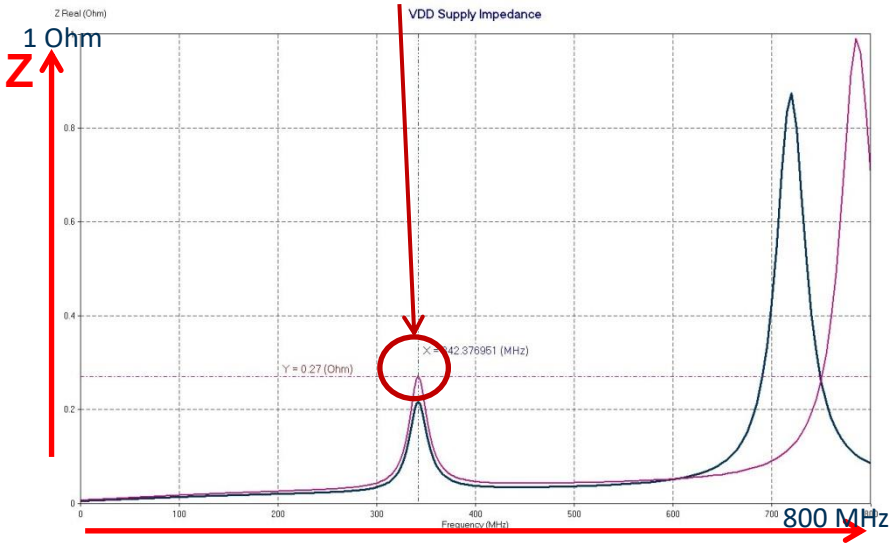
- Simulate PDN (Power Delivery Network) Impedance over Frequency

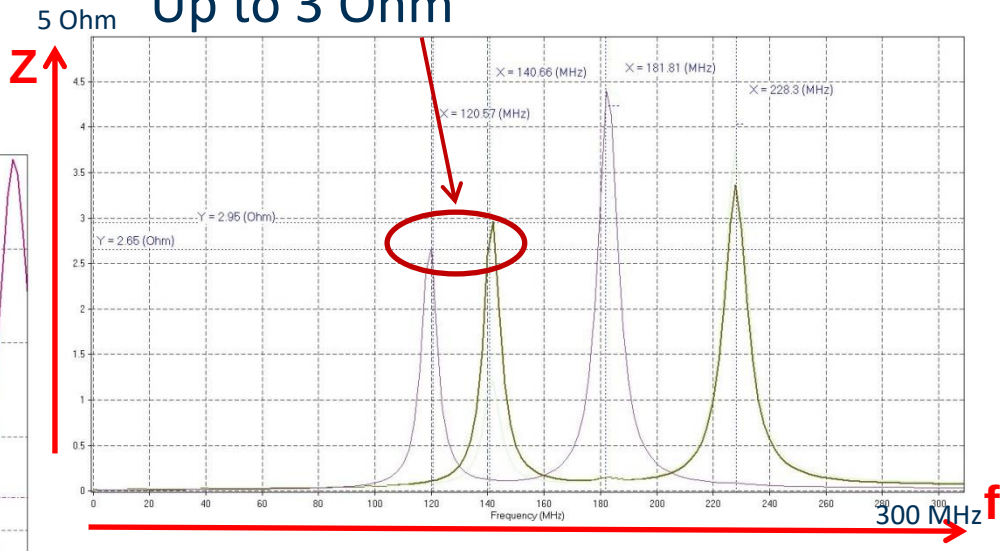
Positive Example

First Resonance @ 340MHz
Only 0.25 Ohm



Negative Example

First Resonances @ 120 – 150 MHz
Up to 3 Ohm



Power Delivery Simulation

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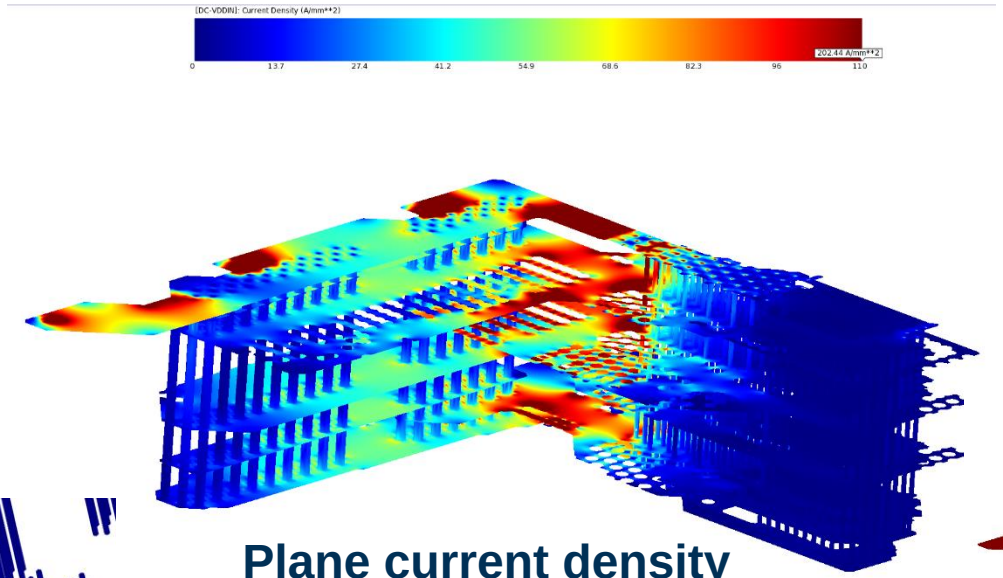
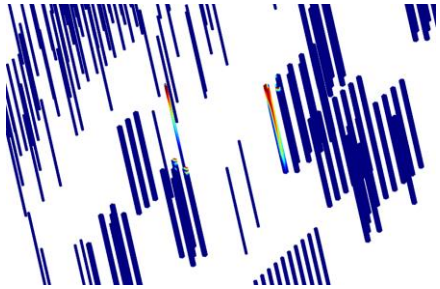
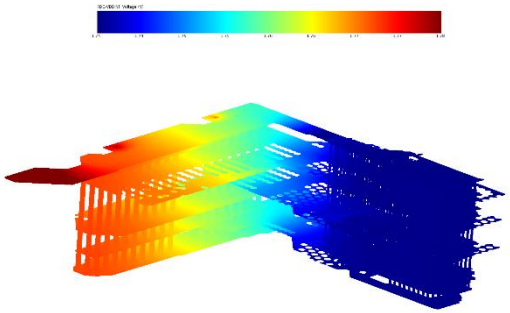
Electro-Thermal simulation considering thermal impact from devices and PCB copper resistance



Plane current density



Via current density

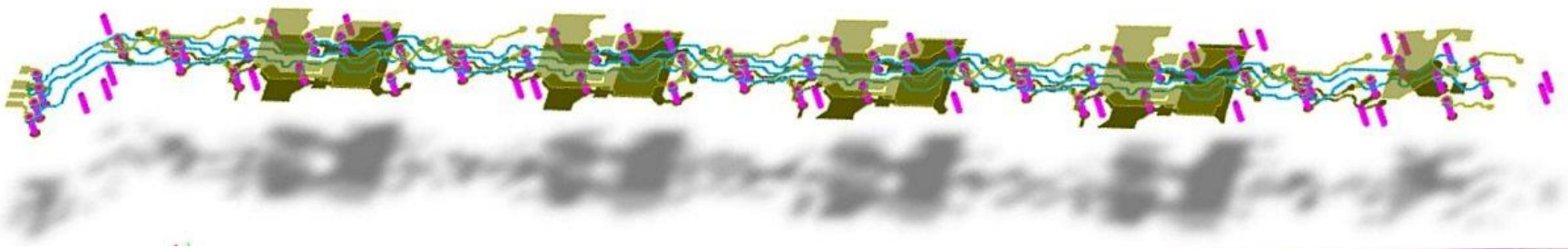


IR Drop of power plane

2.5D Modeling
PCB Layout

- **Cadence and Mentor to ADS Layout Transfer**
- **Simulation in Momentum**
  - Result: S-Parameter Model
  - Co-Simulation with ADS time/frequency Domain Simulation
  - Signal- and Power Supply Integrity
  - Layout accurate Simulation
  - X-talk (intera- and inter layer)
  - Reflections
  - Losses

3 Coupled lines of a CA Bus on a DIMM



3D Modeling
Vias, Packages, Connectors

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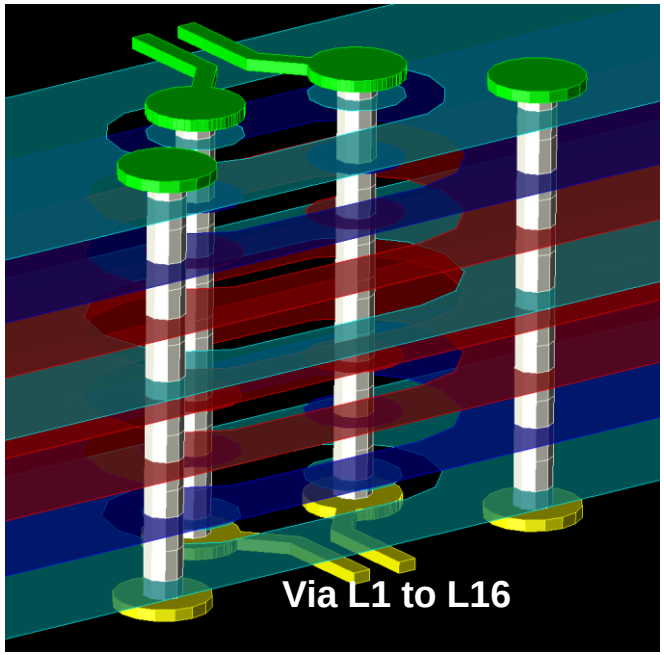
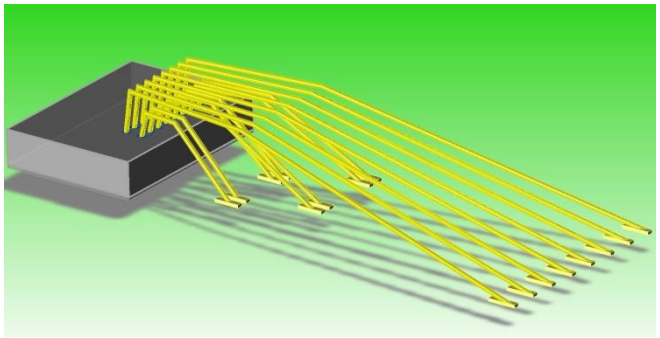
ADS 3D Fieldsolver Momentum and EMDS

- Accurate Via Modeling
- Substrate Routing
- Bondwires
- FBGA Package Balls
- Signal Traces
- Power Planes

Backplane Via





16 coupled Bond Wires:
Signal and Power

Measurement based Modeling
VNA / TDR based

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Characterization of existing boards

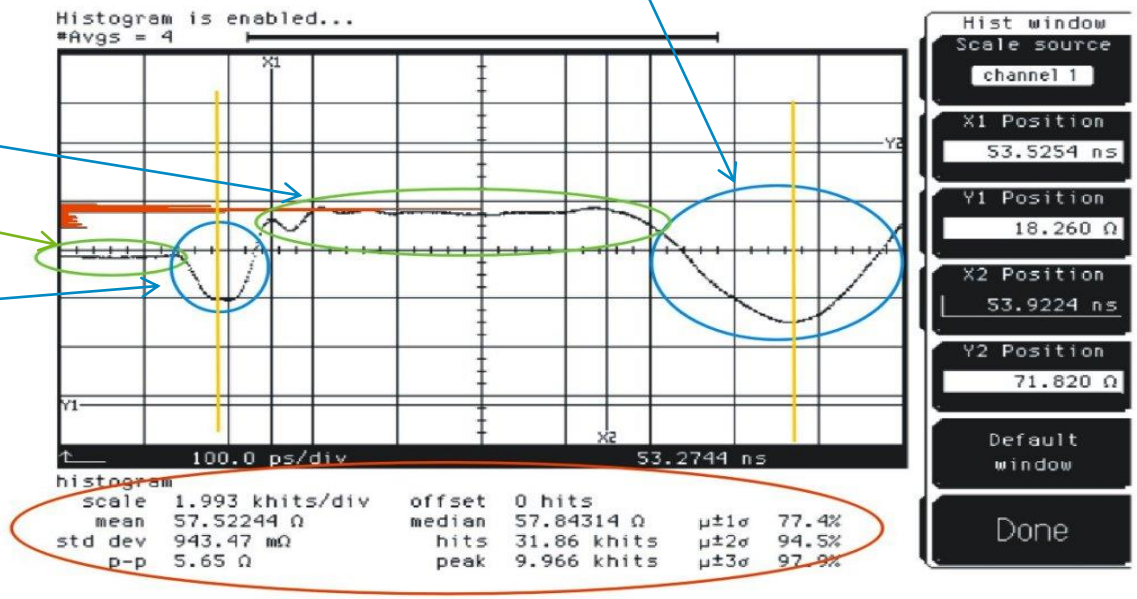
- Measurement with VNA
- TDR/TDT Characterization up to 20 GHz BW

SMD Connector Capacitance

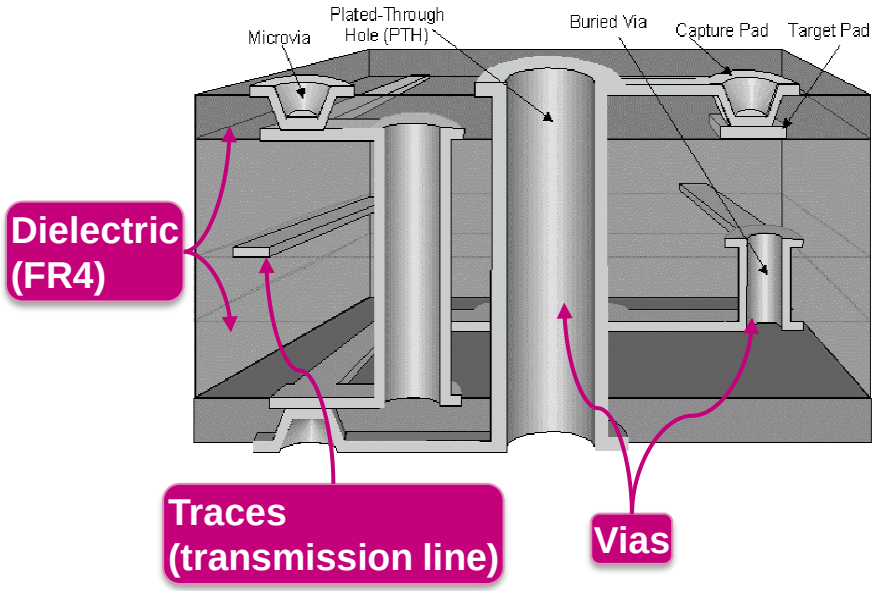
60 Ohm Routing

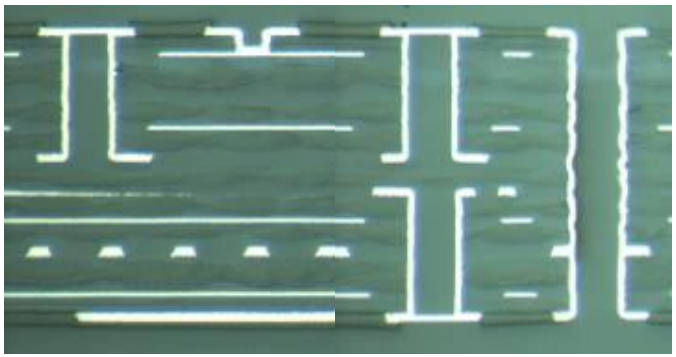
50 Ohm Cable

Pad Capacitance



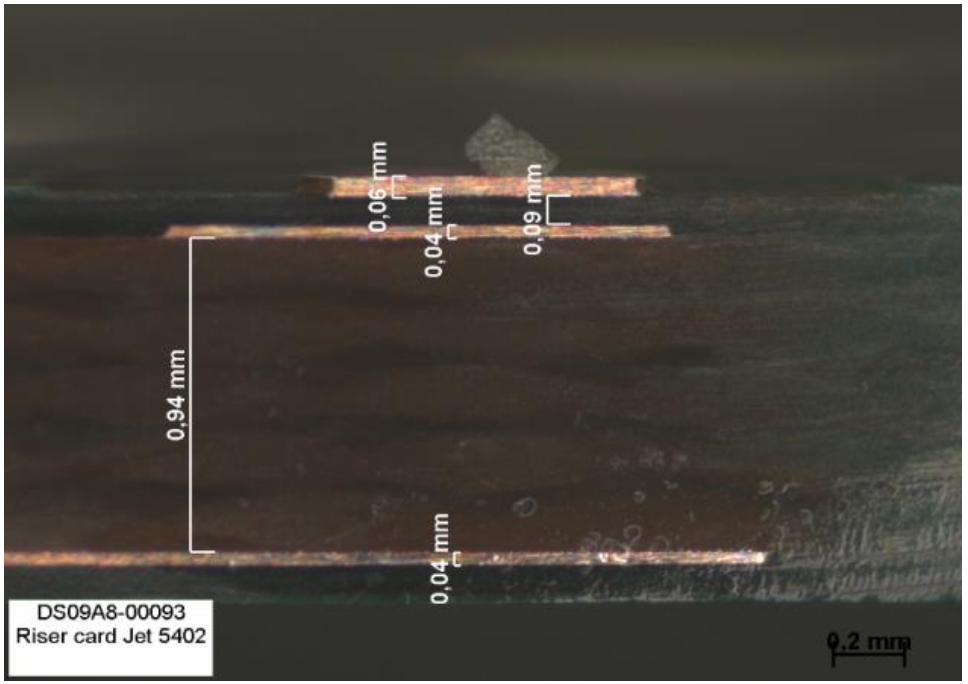
Material Parameter and Modeling
PCB Modeling





Cross section of PCB with blind and micro vias

- Required models for channel simulation:
  - Trace Models
  - Via Models
  - Package Models
  - Connector Models (see next page)



Measurement based Modeling
Testboard Design

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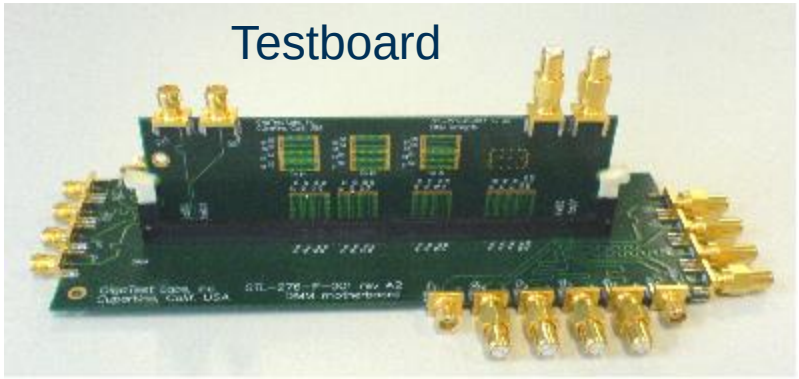
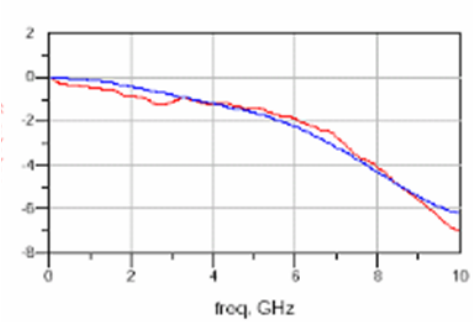
- Definition, Design and Layout of Characterization Boards
- Lumped Model Fitting

Blue: Model
Red: Measurement

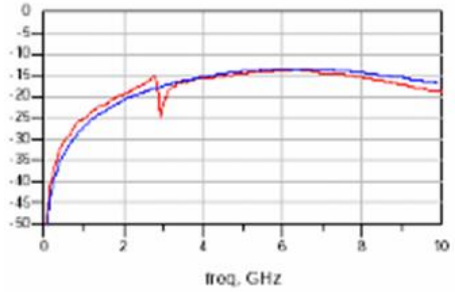
Testboard



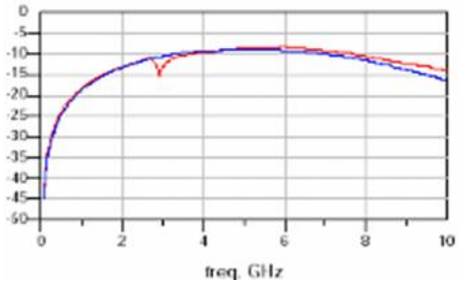
Insertion Loss



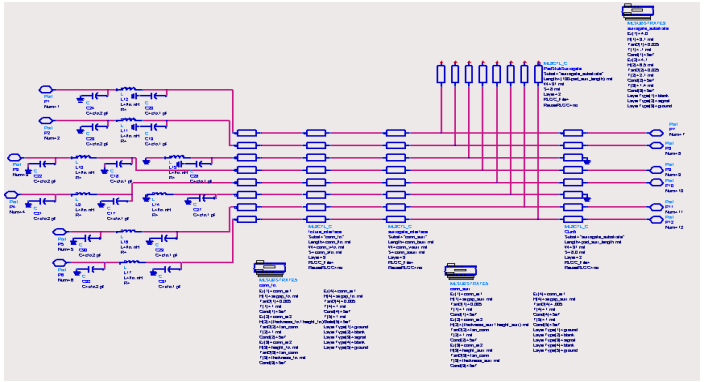
FEXT



NEXT

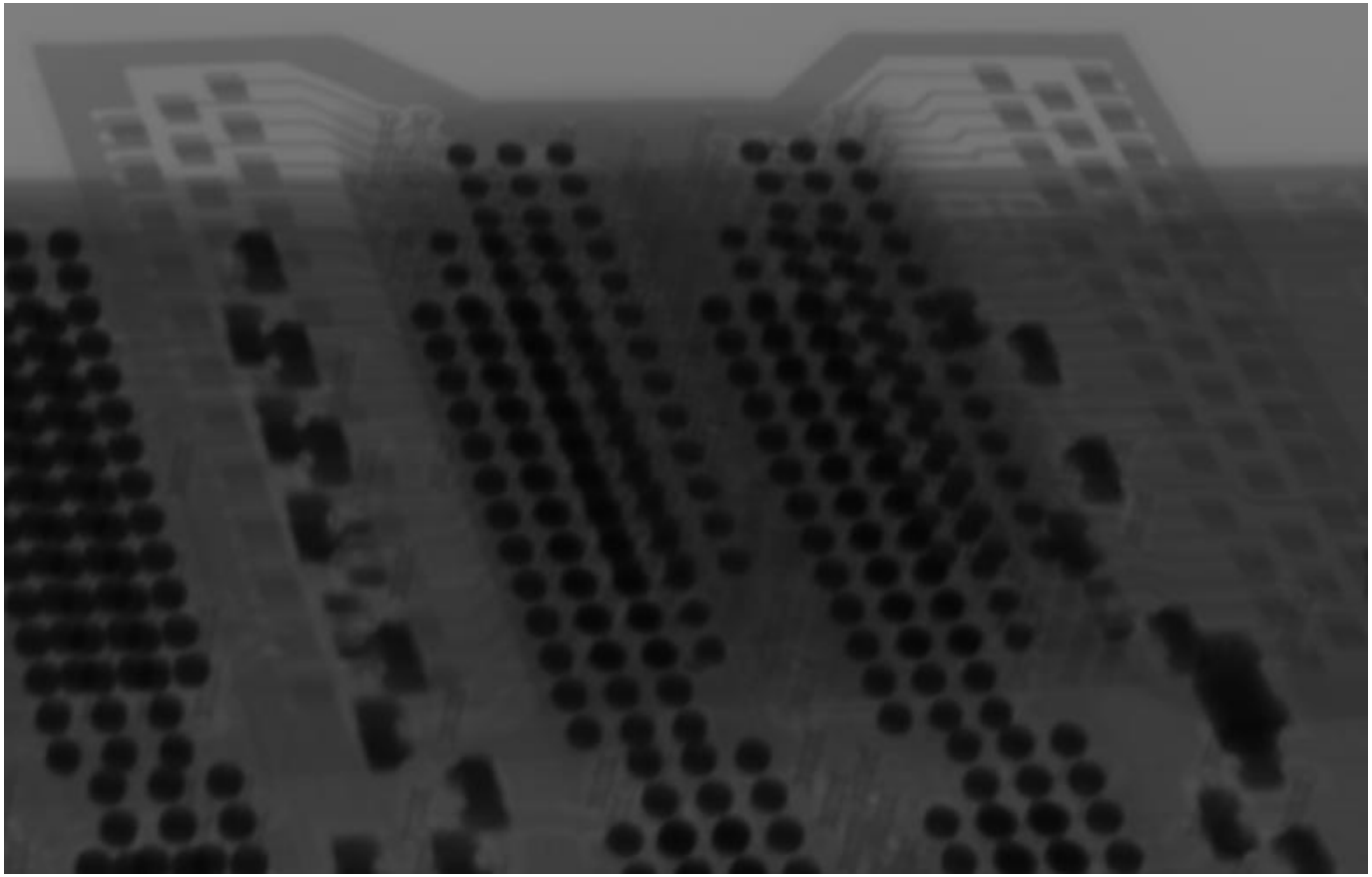


ADS Model fitted to Measurement



Physical Failure analysis

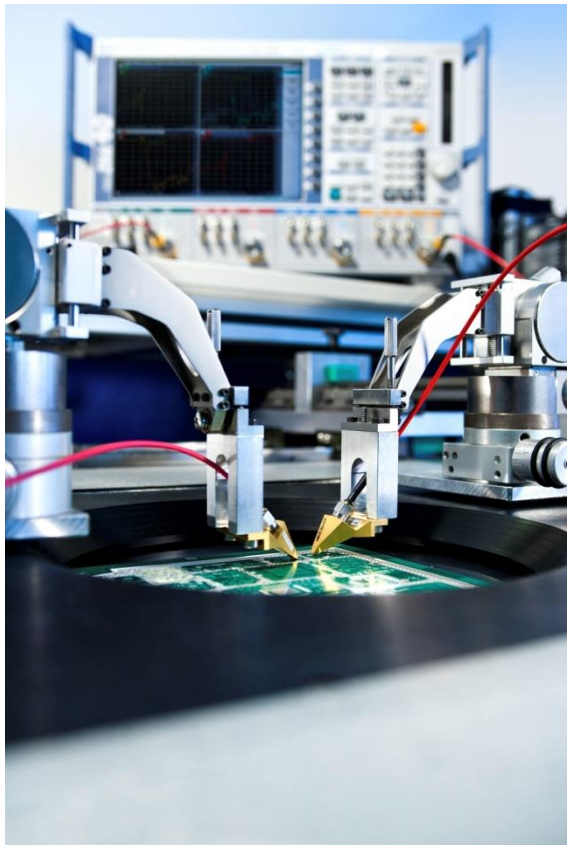
3D CRT



PCB Characterization

Automated Testsystem for PCB characterization up to 110 GHz

- Fully automated to get highly reproducible results
- In cooperation with Rohde & Schwarz



Material Parameter and Modeling
PCB Modeling

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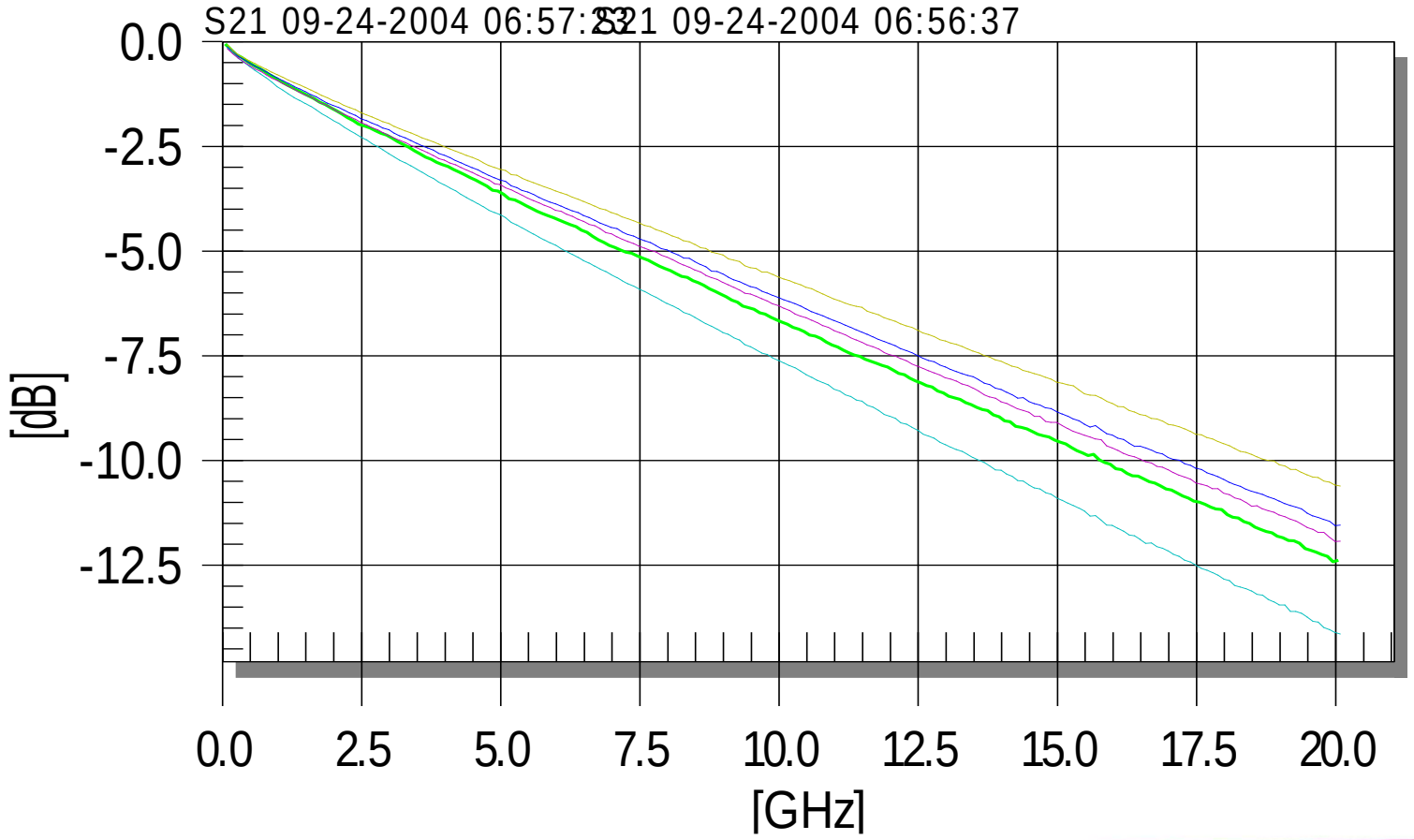
Losses on different PCB materials (MS)



Pre-Compliance Tests

- High Speed Interfaces require verification by Compliance tests.
  - Certified labs offer accredited compliance tests and are required to e. g. use the official logos.
  - If the Logo is not required the alternative is a Pre-Compliance test
- Advantage of Pre-Compliance tests:
  - Deliver not just Pass/Fail, but can be directly starting point of debugging
  - Cheaper as official tests at certified labs
  - Often closer to your location as the next certified lab
- Available Testsetups:
  - PCIe Gen 1 / 2 / 3 / 4 (Equipment capable up to Gen6)
  - SATA Gen 1 / 2 / 3
  - USB Gen 1 / 2 / 3 / 4
  - HDMI
  - DVI
  - Display Port

Pre-Comliance test Examples

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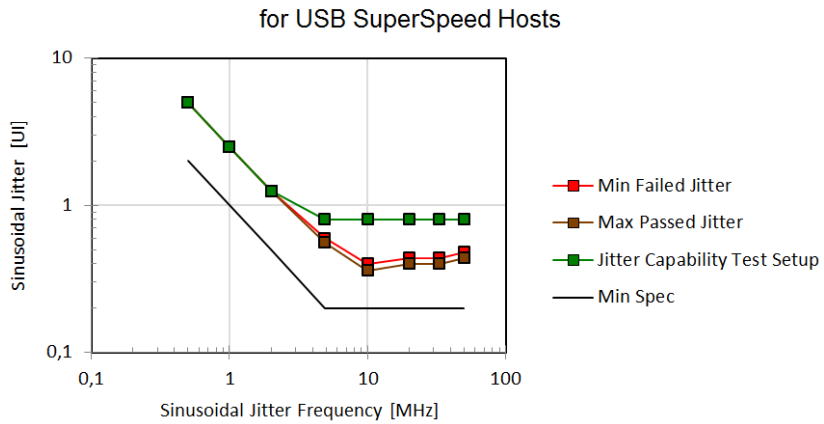
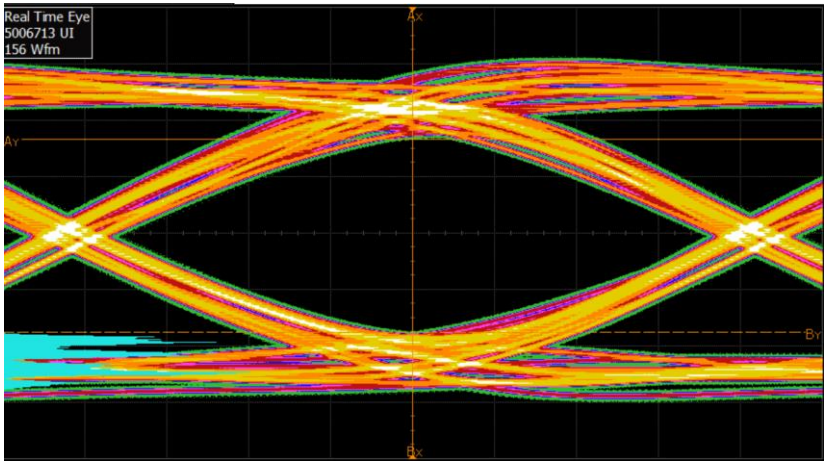
USB3 RX



Test Statistics	
Failed	0
Passed	15
Total	15

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

SATA TX



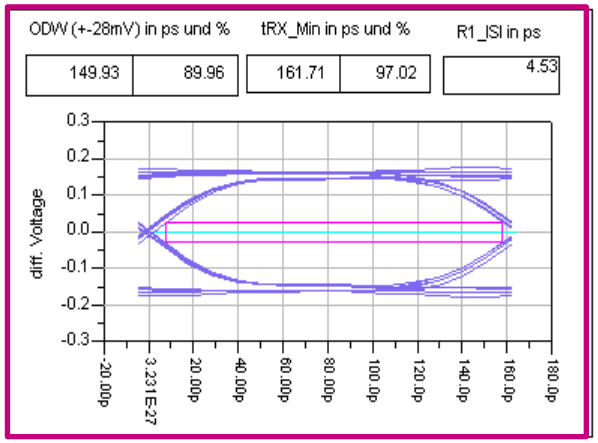
PCIe TX

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	System Board Tx, Unit Interval (PCIE 2.0, 5.0 GT/s)	199.9940 ps	45.0 %	199.9400 ps <= VALUE <= 200.0600 ps
✓	0	1	System Board Tx, Template Tests (PCIE 2.0, 5.0 GT/s)	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	System Board Tx, Peak Differential Output Voltage (PCIE 2.0, 5.0 GT/s)	648.3 mV	38.7 %	300.0 mV <= VALUE <= 1.2000 V
✓	0	1	System Board Tx, Eye-Width w ith crosstalk (PCIE 2.0, 5.0 GT/s)	149.00 ps	56.8 %	VALUE >= 95.00 ps
✓	0	1	System Board Tx, RMS Random Jitter w ith crosstalk (PCIE 2.0, 5.0 GT/s)	2.793 ps	94.2 %	VALUE <= 48.000 ps
✓	0	1	System Board Tx, Maximum Deterministic Jitter w ith crosstalk (PCIE 2.0, 5.0 GT/s)	11.697 ps	79.5 %	VALUE <= 57.000 ps
✓	0	1	System Board Tx, Total Jitter at BER-12 w ith crosstalk (PCIE 2.0, 5.0 GT/s)	50.996 ps	51.4 %	VALUE <= 105.000 ps
✓	0	1	System Board Tx, Eye-Width w ithout crosstalk (PCIE 2.0, 5.0 GT/s)	149.00 ps	38.0 %	VALUE >= 108.00 ps
✓	0	1	System Board Tx, RMS Random Jitter w ithout crosstalk (PCIE 2.0, 5.0 GT/s)	2.793 ps	94.2 %	VALUE <= 48.000 ps
✓	0	1	System Board Tx, Maximum Deterministic Jitter w ithout crosstalk (PCIE 2.0, 5.0 GT/s)	11.697 ps	73.4 %	VALUE <= 44.000 ps
✓	0	1	System Board Tx, Total Jitter at BER-12 w ithout crosstalk (PCIE 2.0, 5.0 GT/s)	50.996 ps	44.6 %	VALUE <= 92.000 ps
✓	0	1	Reference Clock, High frequency > 1.5MHz RMS Jitter (Common Clk) (PCIE 2.0, 5.0 GT/s)	2.21 ps	28.7 %	VALUE <= 3.10 ps
✓	0	1	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk) (PCIE 2.0, 5.0 GT/s)	260 fs	91.3 %	VALUE <= 3.00 ps
✓	0	1	Reference Clock, High frequency > 1.5MHz RMS Jitter (Data Clk) (PCIE 2.0, 5.0 GT/s)	2.54 ps	36.5 %	VALUE <= 4.00 ps
✓	0	1	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clk) (PCIE 2.0, 5.0 GT/s)	340 fs	95.5 %	VALUE <= 7.50 ps

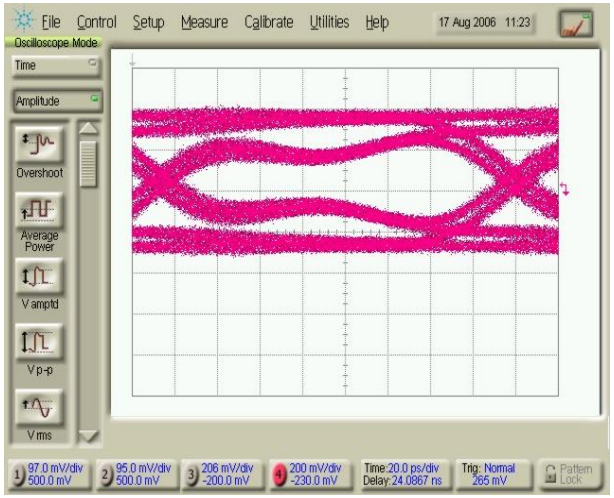
DFT Layout:
Test point placement

Dataeye @ 5.3Gb Measured vs. Simulated / Ball vs. Pad

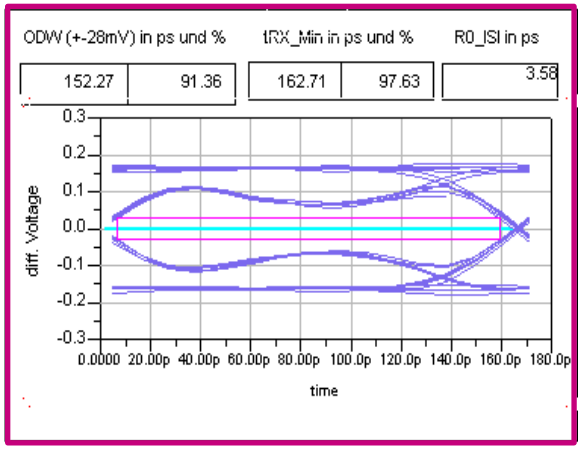
Simulated @ pad



Measurement @ via



Simulated @ via



Logic Analyzer
Digital Timing evaluation

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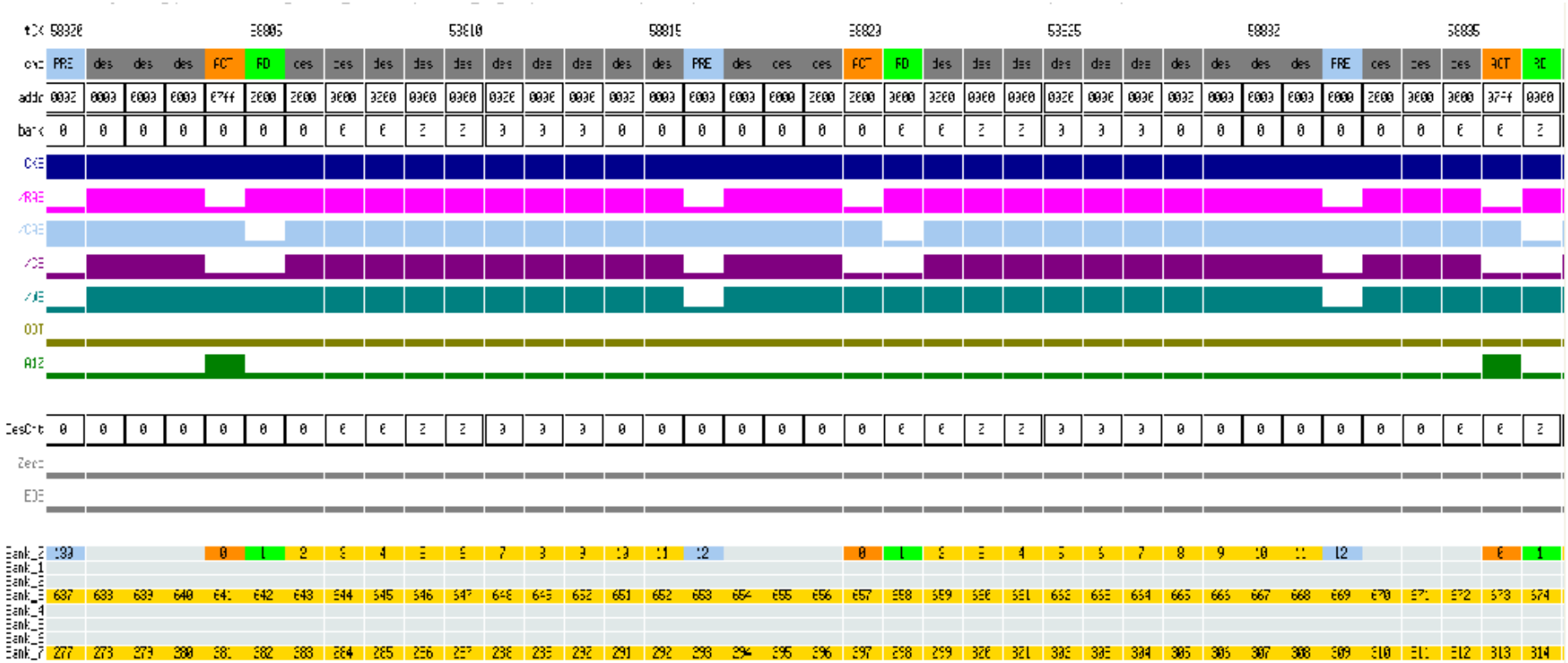
- Spec compliant timings / Finding timing violations
- Digital Timing Settings / MRS setting



Logic Analyzer
Statistical Command sequence evaluation

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- Statistical Access evaluation
- Performance/Power Optimization

Timings:										
AL=3	BL=4	RL=4	TCCD=2	TCK=3750	TFAW=14	TPDN=0	TRAS=12	TRC=16	TRCD=4	TRFC=54
TRP=4	TRRD=3	TRTP=2	TRTW=2	TWR=4	TWTR=2	VDD=1800	WIDTH=64	WL=3	XT=1	

Name	Min	Max
tRAS_bank_0	12	2025
tRAS_bank_1	259	2025
tRAS_bank_2	450	2020
tRAS_bank_3	1874	2030
tRAS_bank_4	-	-
tRAS_bank_5	-	-
tRAS_bank_6	-	-
tRAS_bank_7	573	573
tRAS_rank	12	2030

Name	Min	Max
tRC_bank_0	16	2150
tRC_bank_1	761	2158
tRC_bank_2	718	2182
tRC_bank_3	2032	2122
tRC_bank_4	-	-
tRC_bank_5	-	-
tRC_bank_6	-	-
tRC_bank_7	-	-
tRC_rank	16	2182

Command	Bank_00	Bank_01	Bank_02	Bank_03	Bank_04	Bank_05	Bank_06	Bank_07	Banks_All	TOTAL
RD	1289	402	1180	3884	0	0	0	7	0	6762
WR	1107	402	0	7	0	0	0	4	0	1520
ACT	45	31	31	30	0	0	0	1	0	138
RD_AP	0	0	0	0	0	0	0	0	0	0
WR_AP	0	0	0	0	0	0	0	0	0	0
PRE	16	2	2	1	0	0	0	1	0	22
PRE_A	0	0	0	0	0	0	0	0	30	30
des	0	0	0	0	0	0	0	0	55843	55843
nop	0	0	0	0	0	0	0	0	0	0
MRS	0	0	0	0	0	0	0	0	0	0
REF	0	0	0	0	0	0	0	0	31	31
SRE	0	0	0	0	0	0	0	0	0	0
SRX	0	0	0	0	0	0	0	0	0	0
PDE	0	0	0	0	0	0	0	0	0	0
PDX	0	0	0	0	0	0	0	0	0	0
PRE_I	0	0	0	0	0	0	0	0	0	0
PDCONT	0	0	0	0	0	0	0	0	0	0
BST	0	0	0	0	0	0	0	0	0	0
DPD	0	0	0	0	0	0	0	0	0	0

tRCD_bank_0	1	5
tRCD_bank_1	1	11
tRCD_bank_2	1	6
tRCD_bank_3	1	10
tRCD_bank_4	-	-
tRCD_bank_5	-	-
tRCD_bank_6	-	-
tRCD_bank_7	5	5
tRCD_rank	1	11

tRP_bank_0*	4	124
tRP_bank_1*	5	1763
tRP_bank_2*	5	268
tRP_bank_3*	5	142
tRP_bank_4*	-	-
tRP_bank_5*	-	-
tRP_bank_6*	-	-
tRP_bank_7*	1089	1089
tRP_rank	4	1763

tRFC	55	55
tREFI	2072	2091
tRRD	3	2070
tCCD	2	77

Failure Analysis
Software Memory test: Decoding

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

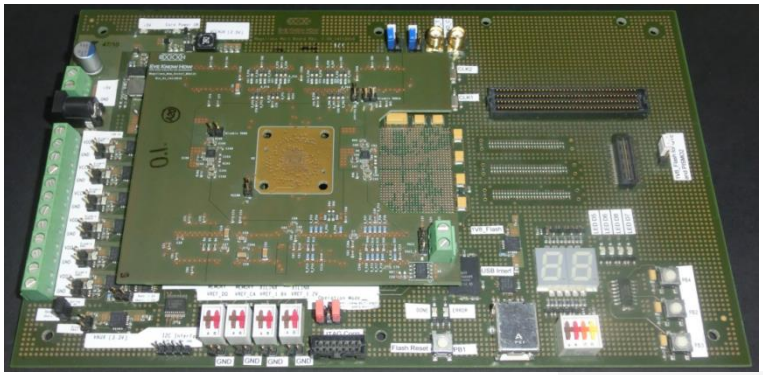
- Memory test failure Analysis
  - Evaluate log files from Software Memory tests
  - Narrow down failure reason
  - DQ vs. CA related fail
  - Single DQ vs. DQS fail
  - Read vs. Write fail
  - Device vs. Signal integrity related fail
  - Vref Margin test implementation
  - Adjust VREF until fail and evaluate fail behavior
  - Timing Margin test implementation
  - Change Controller delays (DQS and CLK) until fail and evaluate fail behavior

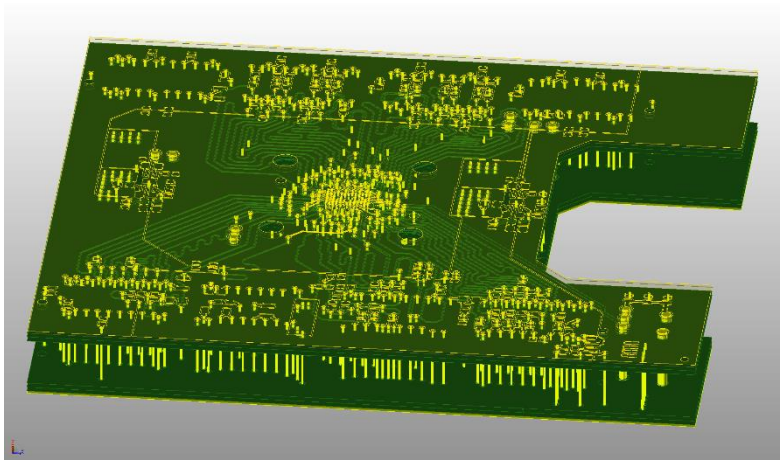
12742808	12742822
FAILURE: possible bad address line at offset 0x00000000 = address 0x099C0038 Expected value F663FFC7, Read value 099C0038 Re-Read: Expected value F663FFC7, Read value 099C0038 Expected value F663FFC7, Read value 099C0038 Expected value F663FFC7, Read value 099C0038 Expected value F663FFC7, Read value 099C0038	FAILURE: possible bad address line at offset 0x018A5141 = address 0x062D4504 Expected value F9D2BAFB, Read value 8002BAFB Re-Read: Expected value F9D2BAFB, Read value 8002BAFB Expected value F9D2BAFB, Read value 8002BAFB Expected value F9D2BAFB, Read value 8002BAFB Expected value F9D2BAFB, Read value 8002BAFB Skipping to next test...

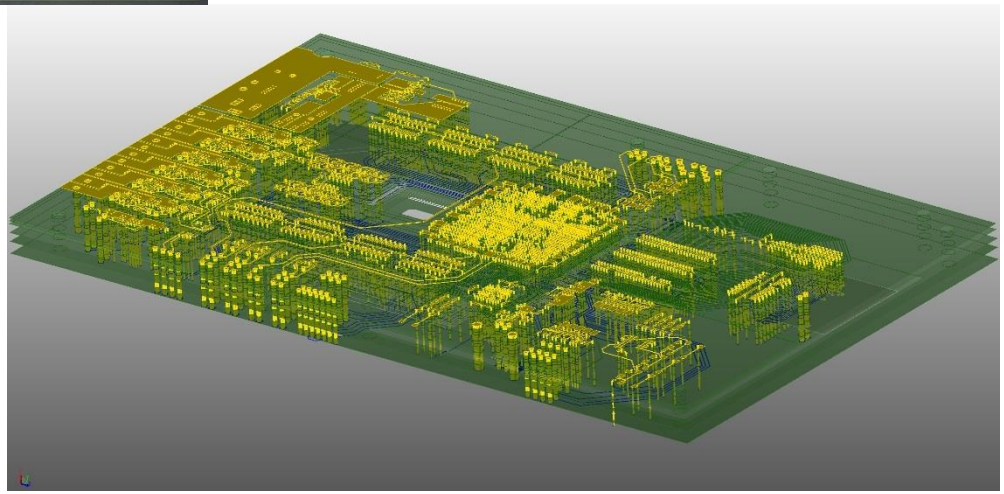
Design and Layout
Xilinx FPGA based Test board

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

DRAM Characterization Testboard

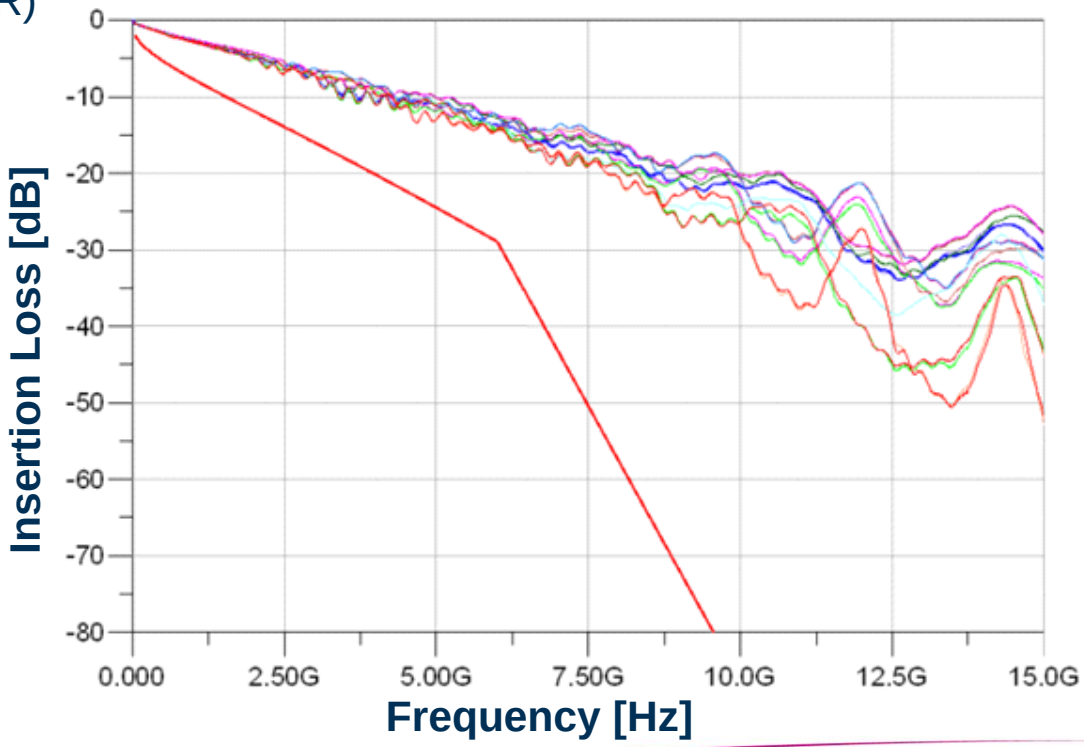






Layout and Design optimization Example: Backplane 10G Spec

- Simulate and measure Backplane e. g. 10G Base – KR
  - Fitted Attenuation (FA)
  - Insertion Loss (IL)
  - Insertion Loss Deviation (ILD)
  - Insertion Loss to X-talk (ICR)

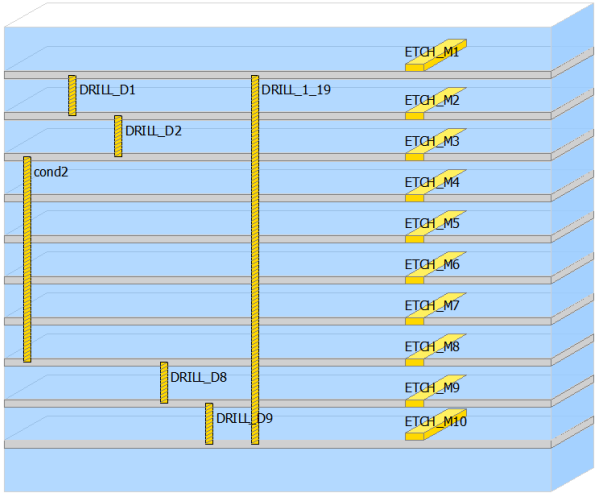


Physical optimization for High speed Signaling

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

Stackup Design

- HDI proven and high speed Stackup
- High speed material



Routing Design

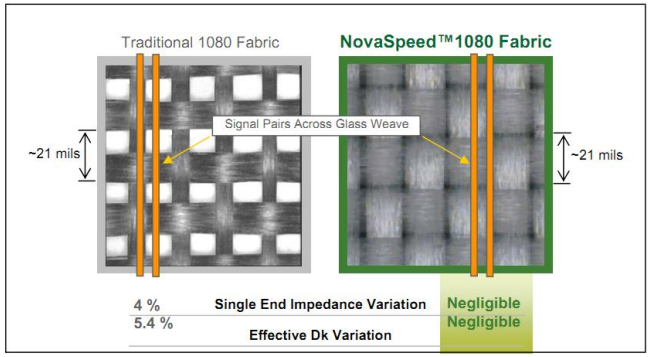


Figure 4: Improved signal integrity and clock rate.

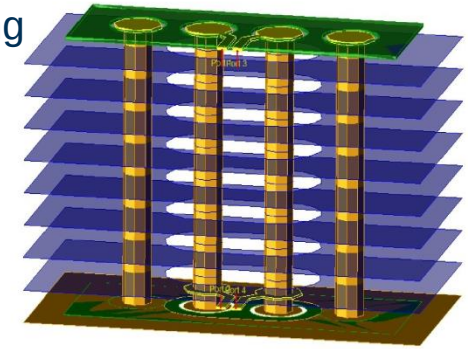
Presented at the
HyperTransport™ Technology Developers Conference
October 2007

Advanced Glass Reinforcement Technology for Improved Signal Integrity

By
Russell Dudek, Compunetics, Inc.
Patricia Goldman & John Kuhn, Dielectric Solutions, LLC

Via Design

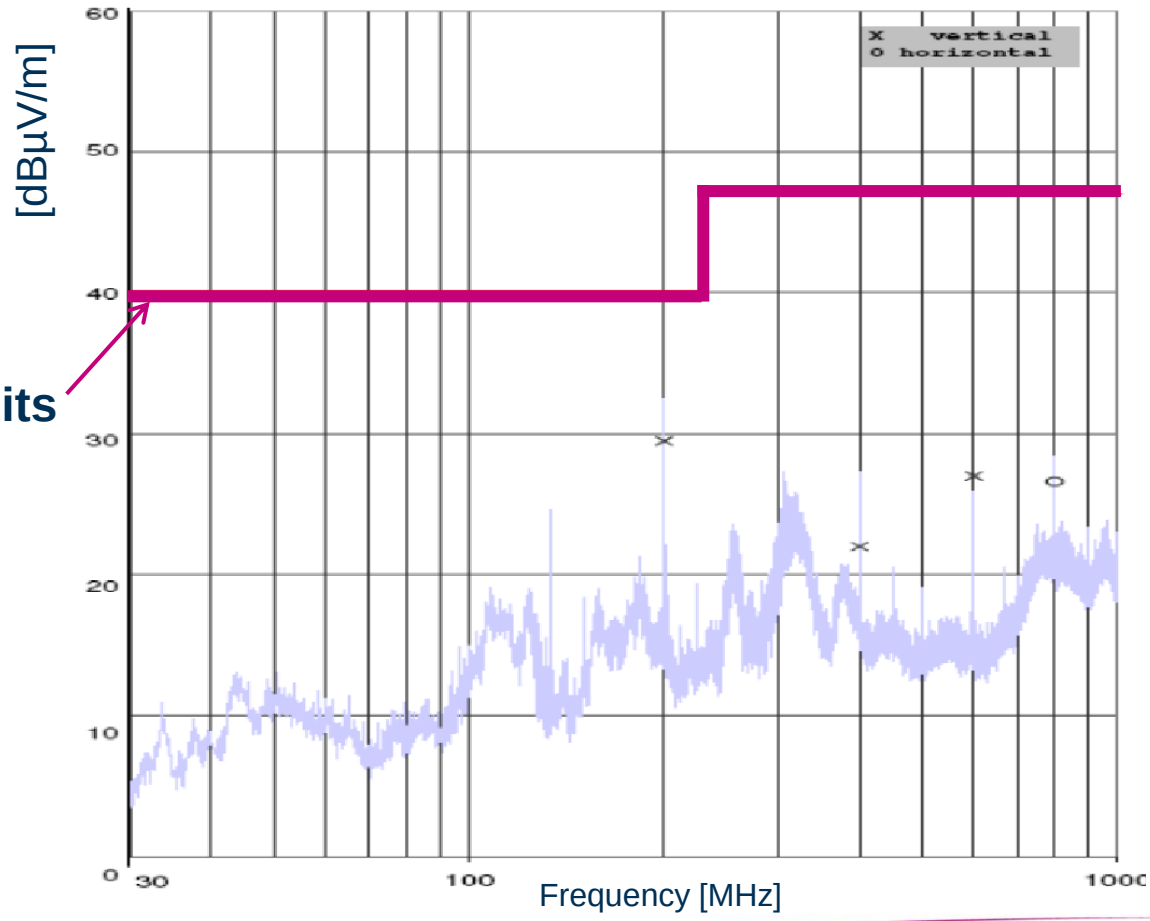
- Optimize via to 100 Ohm
- Optimize connector pin field:
  Via + BreakOut Routing



EMI/EMC consulting

Interference Radiation Test

System Specification Limits (e.g. for PC, Server)



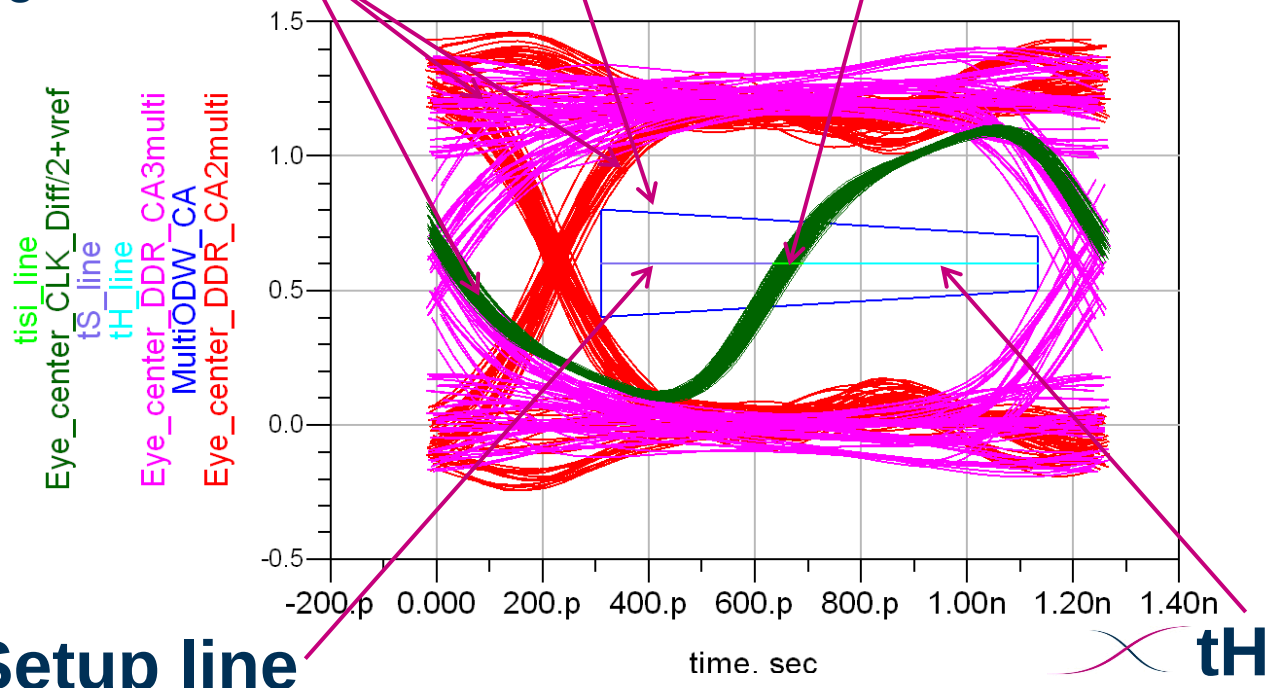
Data Evaluation
EKH ael DRAM Eye routines

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

ODW: Multi Signal open Data Window

ISI line

Multiple Eyes incl. Timing Reference



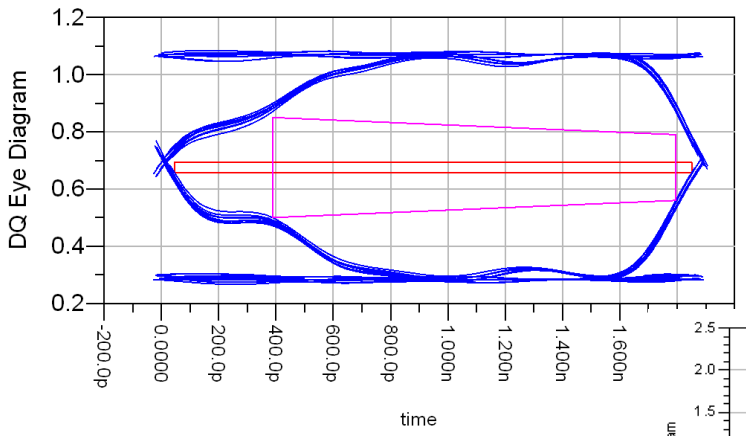
tSetup line

tHold line

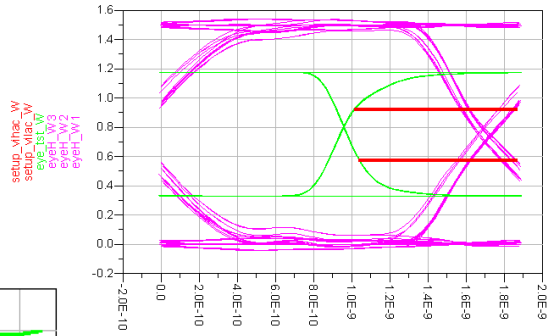
Examples with some Details: EKH Eye visualization

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

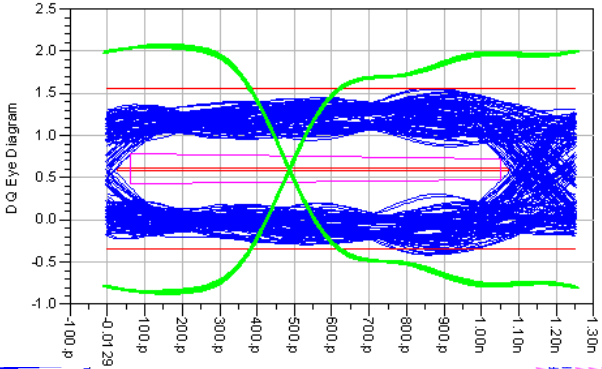
AC/DC based eye aperture



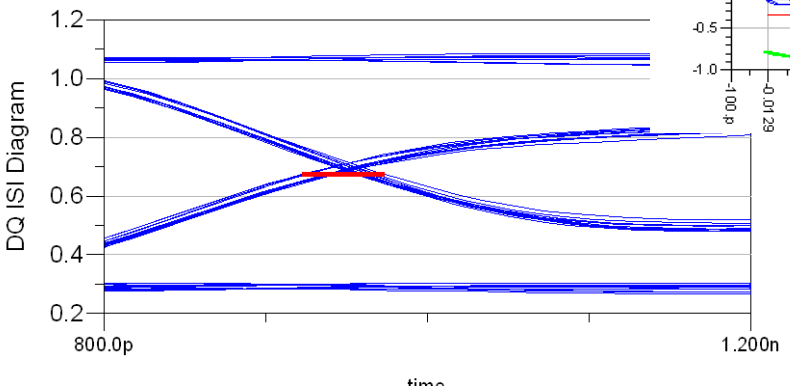
Flight time based timing calculation



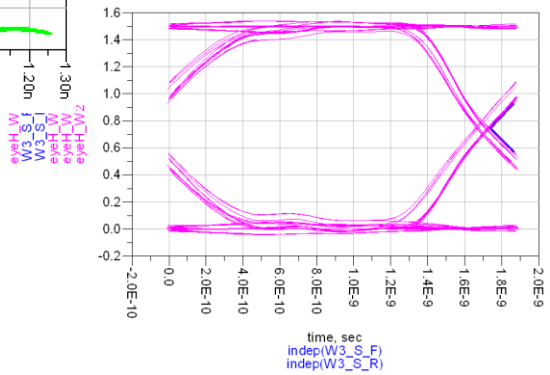
Eye Overlay



ISI at Vref

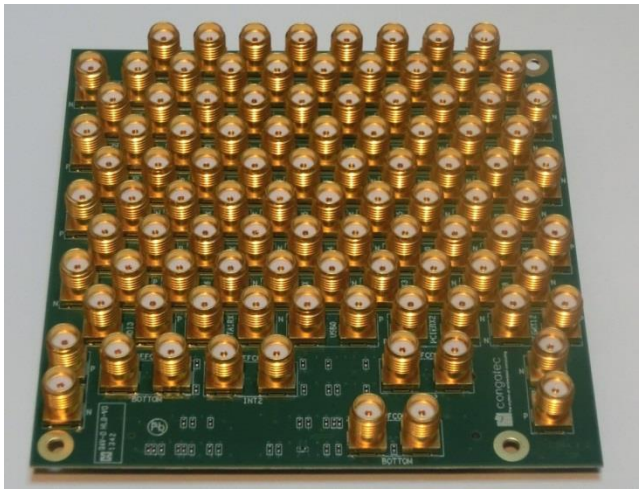


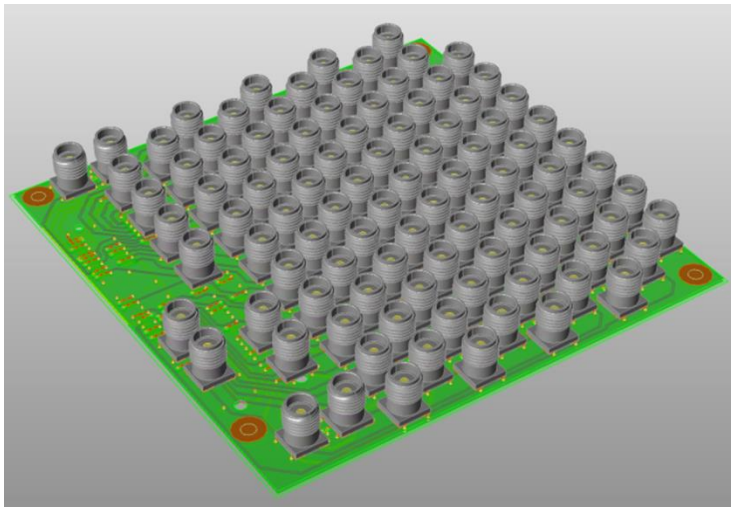
Slew Rates



ComExpress
Carrier Board Characterization

- Unique Testboard for direct connection to high speed traces on ComExpress Carrier board





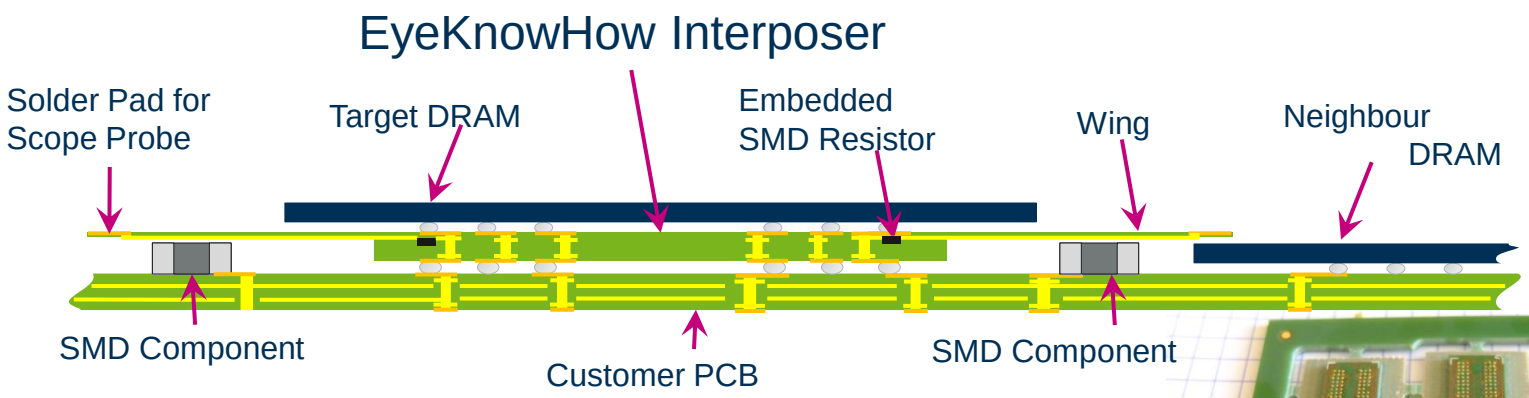
- Simulated and optimized up to 20GHz
- Improved Material
- All high speed lanes connected to SMA
- De-embedding of Test Fixture possible

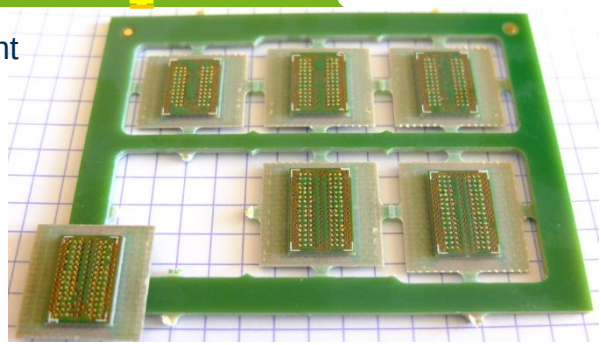
Memory Interposer for DRAM Compliance Testing

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

Available as Service or Product

- For DDR2/3/4/5, x4/x8/16, Planar or Stacked
- LPDDR4/5 x32 (200 Ball package)





High Performance, Low Parasitic's

- Can be de-embedded
- Wing Design for flexible usage with maximum DRAM size and minimum Board spacing
- High accurate embedded resistors