7 to10 GHz and 14 to 20 GHz FMCW Modulator for RADAR

1 Features

QFN40 6mm X 6mm
Ultra-Linear Ultra-Fast FMCW Chirp Generator
Ultra Low PN (SSB): -108 dBc/Hz at Δf = 1 MHz (1)
Reference input: 20 MHz to 200 MHz
Power Dissipation: 750 mW(2) / 390 mW(3)
Output frequency range:
- 7.0 GHz to 10.13 GHz
- 14.0 GHz to 20.25 GHz

Chirp modulation BW: 1.4 GHz typ., 1.1GHz min. (1)
Excellent linearity: INL < 0.2% typ.
Chirp up / retrace slopes: 200 / 500 MHz/us (1)
Retrace time: < 0.5 us / 2 us @ BW 125 / 1000 MHz (1)
Negligible undershoot < 0.5% Chirping Bandwidth
Lock time: < 5 us (2)
No lock loss for 1 GHz linear frequency jump within 1 us
Programmable Chirp Profiles
Bank of LC-VCOs with 128 Bands/VCO
Automatic VCO/Band Selection System
Built-in auto calibration over process and temperature
Analog Test Bus functionality for real-time FuSa functionality

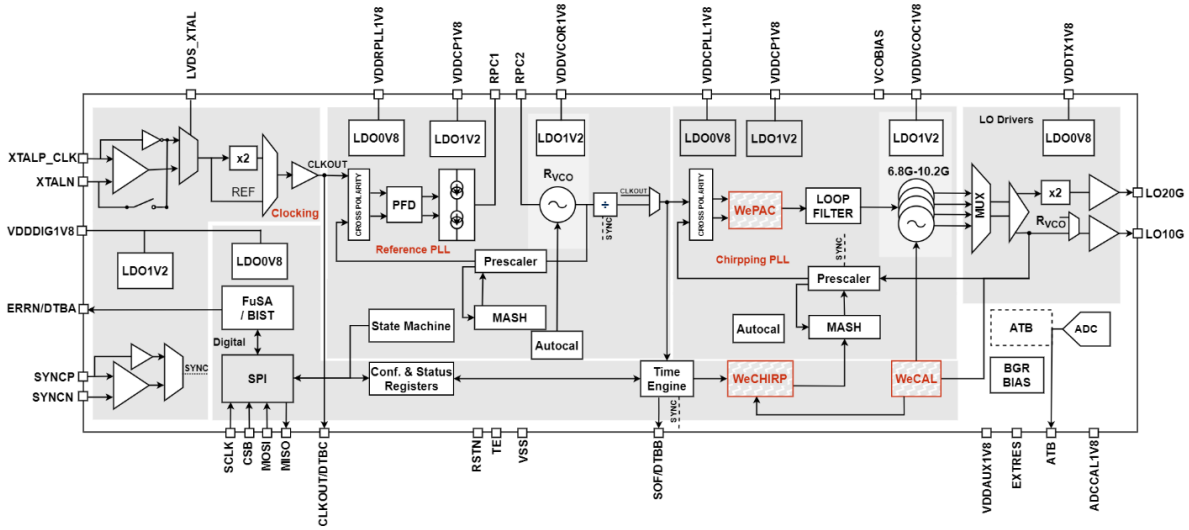
2 Applications

Radar applications
Automotive FMCW Radars

3 Description

The WEA520SFMCW22G is an ultra-fast ultra-linear FMCW frequency synthesizer capable of generating 1400 MHz Chirps at 20 GHz frequency. It uses a reference input ranging from 20 MHz to 200 MHz, with the use of an external Crystal or clock (CMOS or LVDS). The WEA520SFMCW22G generates an RF signal spanning from 7.0 GHz up to 20.25 GHz with the four integrated VCOs and the use of an RF frequency doubler and divider. The synthesizer utilizes the WEASIC proprietary WeCHIRP™, wePAC™, weCAL™ technologies to provide very fast ramp retracing and settling times while maintaining industry leading phase noise during chirping. The modulator has a phase synchronization capability for coherent operation with other modulators. It also provides synchronized trigger event signals for the RADAR Transmitter and Receiver chips. By the use of internal high PSRR LDOs, the WEA520SFMCW22G can withstand noisy power supply environment. It is powered by a single 1.8 V supply

Simplified Schematic



(1) at 20GHz, (2) All Output paths Powered On, (3) Only 20GHz Path Powered On

Table of Contents

4 Revision History

12/2024 – Revision v1.0: Initial version

2/2025 - 6.2 Performance table updated

5. Pin Configuration and Function Description

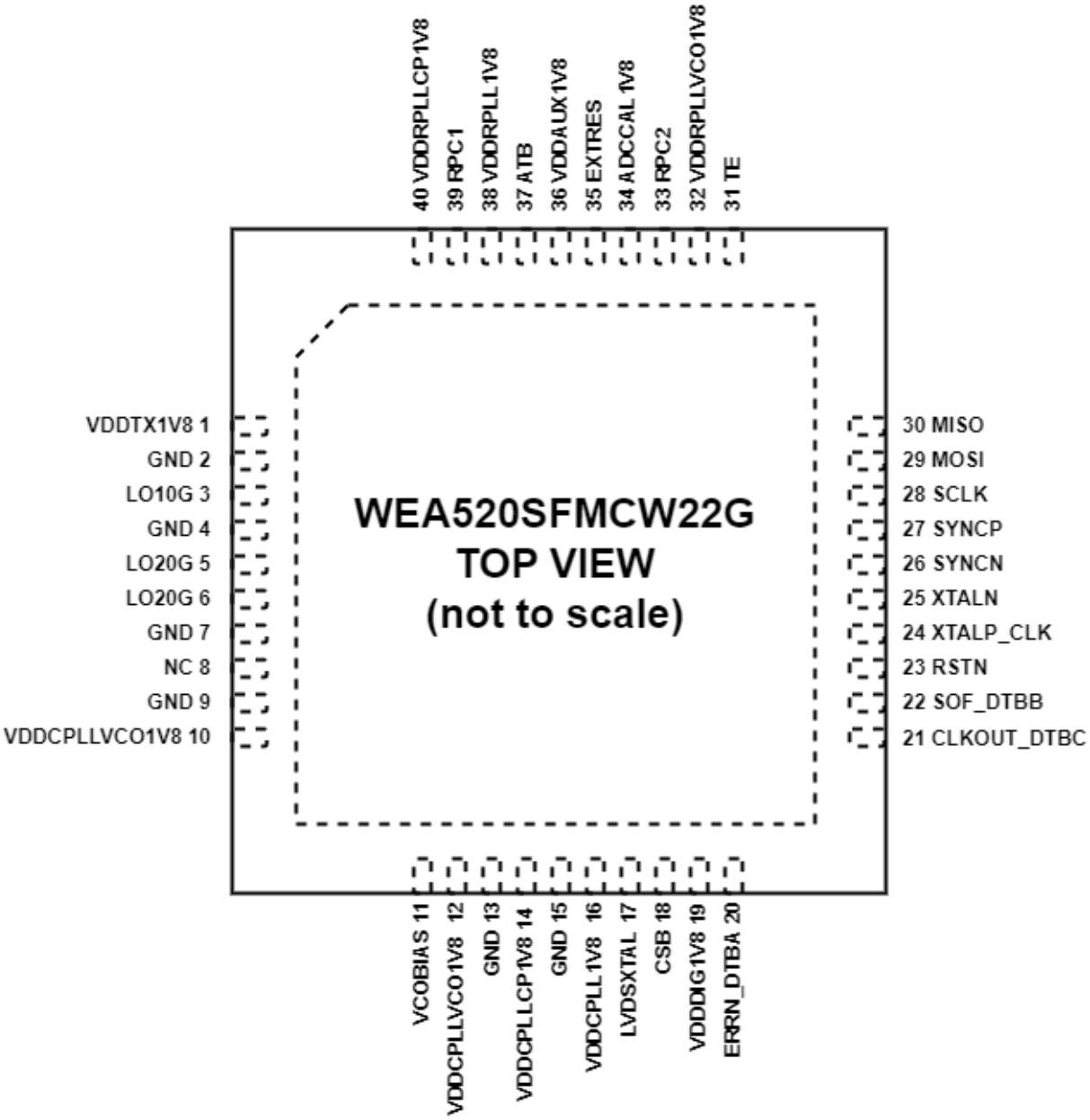


Figure 1. Pin-Out Configuration

5.1 Pin Function Descriptions

PIN		I/O	DESCRIPTION
No.	Name		
34	ADCCAL1V8	Bias	ADC calibration voltage (1.8 V - 0.1% accuracy)
37	ATB	Output	Analog Test Bus
21	CLKOUT_DTBC	Output	CLOCK OUT Digital Test Bus C
18	CSB	Input	SPI Chip Select (Active Low)
20	ERRN_DTBA	Output	Interrupt Request Digital Test Bus (DTB) A
35	EXTRES	Bias	External resistor reference (bias calibration)
2,4,7,9,13,15	GND	Ground	Ground
8		NC	
5,6	LO20G	Output	Chirping Synthesizer Frequency Doubled RF output
3	LO10G	Output	Chirping Synthesizer RF output
17	LVDS_XTAL	Input	CLOCK topology input selector LVDS/BUFFER-OSCILLATOR
30	MISO	Output	SPI Master In Slave Out
29	MOSI	Input	SPI Master Out Slave In
39	RPC1	Loop Filter	Reference PLL Charge Pump output
33	RPC2	Loop Filter	Reference PLL VCO input
23	RSTN	Input	Reset (Active Low)
28	SCLK	Input	SPI clock
22	SOF_DTBB	Output	Synchronized Output Frame Digital Test Bus (DTB) B
26	SYNCN	Input	SYNC IN LVDS (-)
27	SYNCP	Input	SYNC IN LVDS (+) SYNC IN Buffer
31	TE	Input	Test Enable

11	VCOBIAS	Bias	VCO Bias
36	VDDAUX1V8	Supply	Bias / ADC 1.8 V supply
14	VDDCPLLCP1V8	Supply	CPLL Charge Pump 1.8 V supply
40	VDDRPLLCP1V8	Supply	RPLL Charge Pump 1.8 V supply
19	VDDDIG1V8	Supply	Logic/IO 1.8 V supply
16	VDDCPLL1V8	Supply	CPLL 1.8 V supply
38	VDDRPLL1V8	Supply	RPLL 1.8 V supply
1	VDDTX1V8	Supply	LO generation path 1.8 V supply
10,12	VDDCPLLVCO1V8	Supply	CPLL VCO 1.8 V supply
32	VDDRPLLVCO1V8	Supply	RPLL VCO 1.8 V supply
25	XTALN	Input	LVDS IN N (-) Crystal oscillator output
24	XTALP_CLK	Input	LVDS IN P (+) Crystal oscillator input External reference input (0/1.8 V Logic)

6 Specifications

6.1 Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage	1.7	1.8	2.0	V
Total Power consumption		750		mW
VDDAUX1V8		7		mA
VDDDIG1V8 (digital consumption not included)		26		mA
VDDTX1V8		110		mA
VDDPLL1V8 RPLL		14		mA
VDDPLL1V8 CPLL		26		mA
VDDCP1V8 RPLL		22		mA

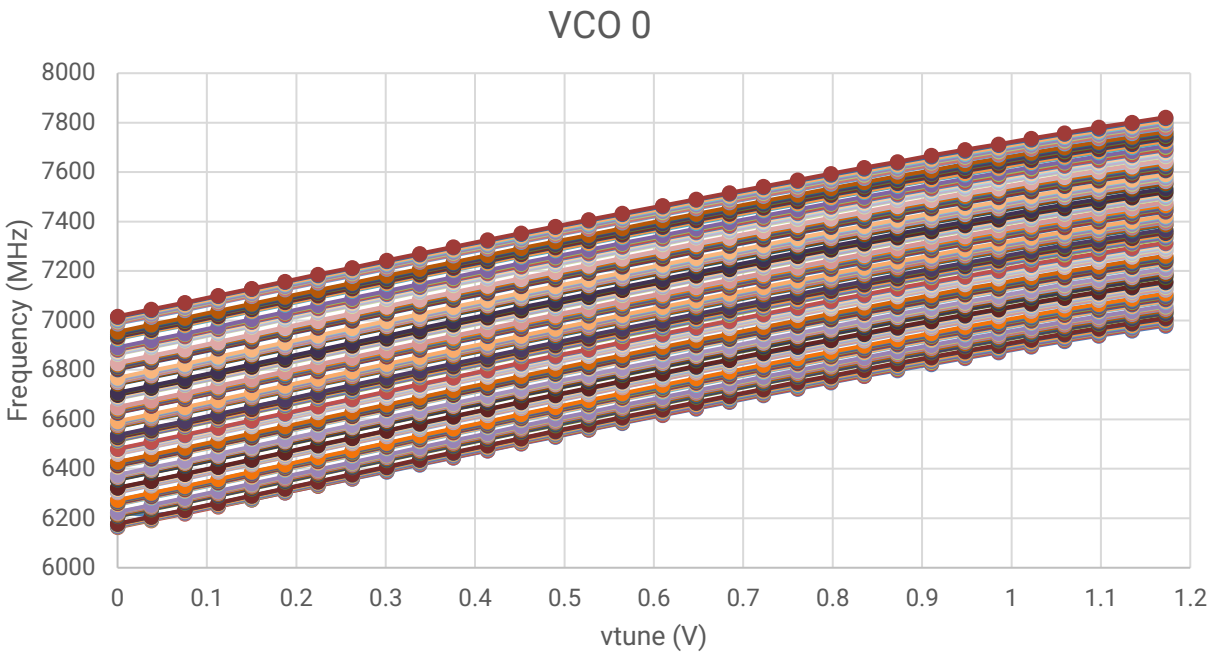
VDDCP1V8 CPLL		62		mA
VDDVCO1V8 RPLL		56		mA
VDDVCO1V8 CPLL		85		mA
Ambient Temperature	-40		125	oC

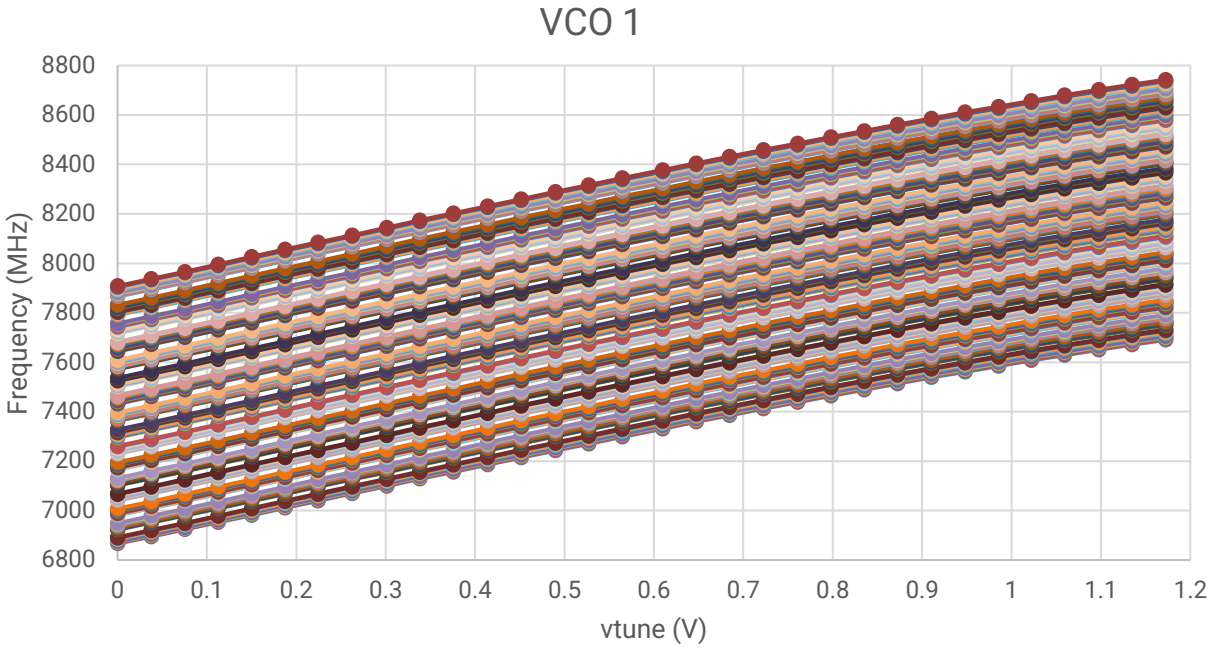
6.2 Performance

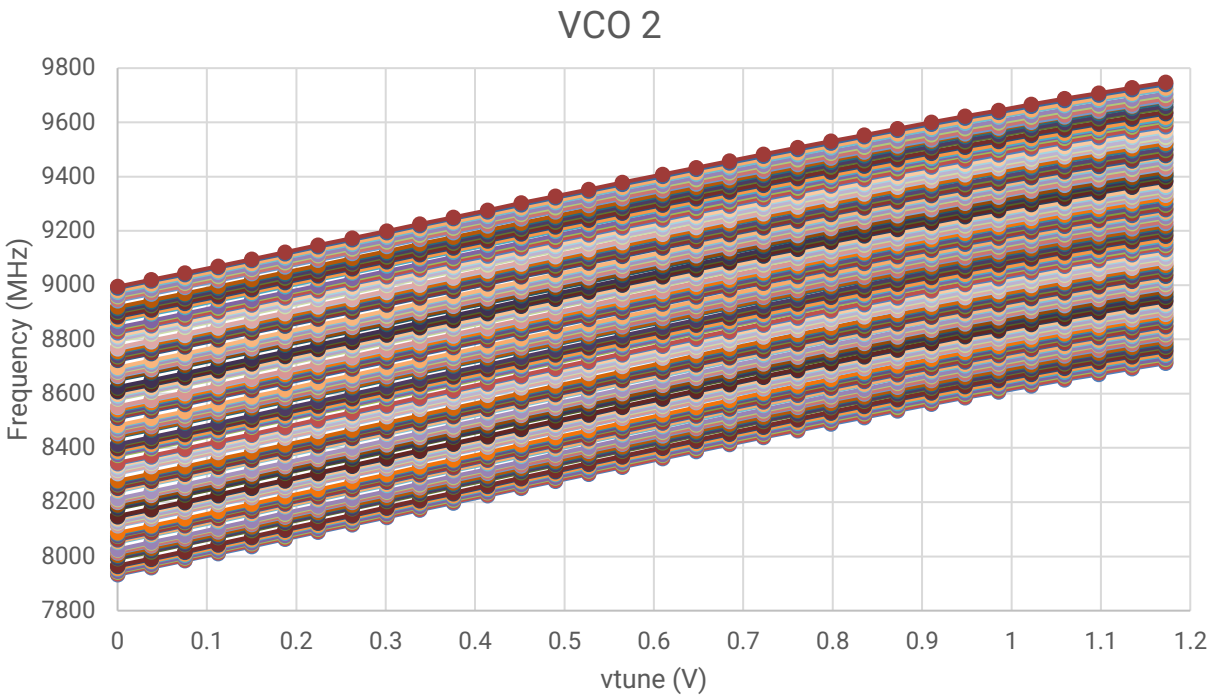
Metrics	Min	Typ	Max	Units
REF PLL				
Minimum Frequency		6.10		GHz
Maximum Frequency		7.40		GHz
VCO Tuning Range	35.1	49.1	70.9	MHz
VCO tuning sensitivity (Kv) - median	58.53	81.83	118.15	MHz/V
VCO pushing		-390.75		kHz/V
VCO temperature sensitivity		-479.81		KHz/°C
VCO number of Bands		256		
Input reference	20.0		200	MHz
Loop Bandwidth		100		KHz
MASH order		2^{nd} or 3^{rd}		
Charge Pump Programmable Current	1		4.5	mA

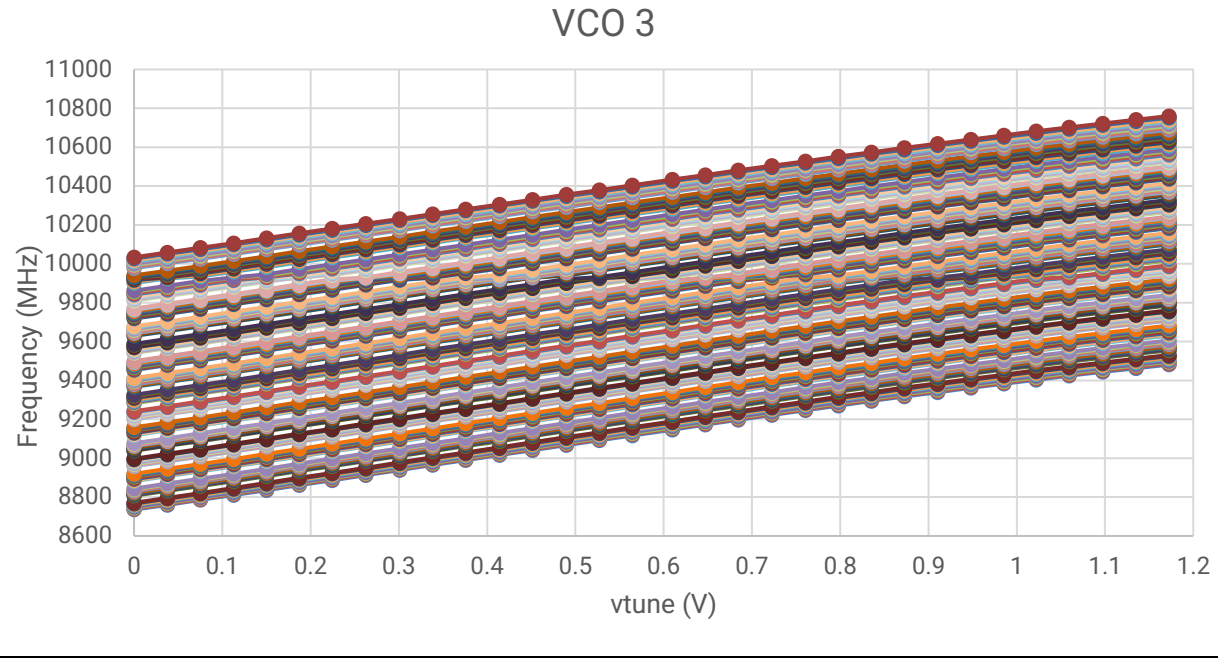
CHIRP_PLL

VCO Tuning Range (BW)

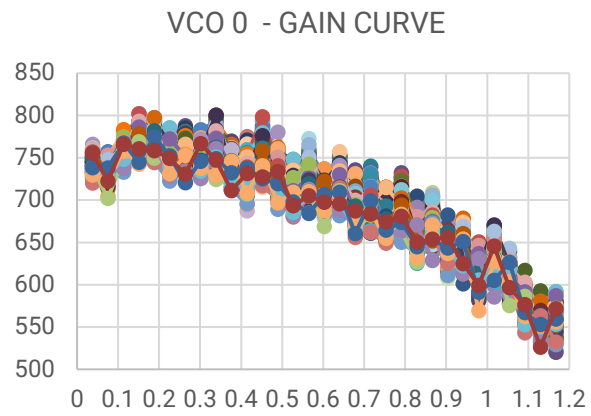


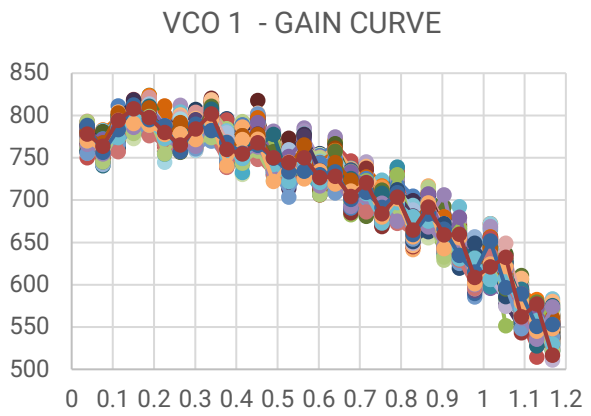


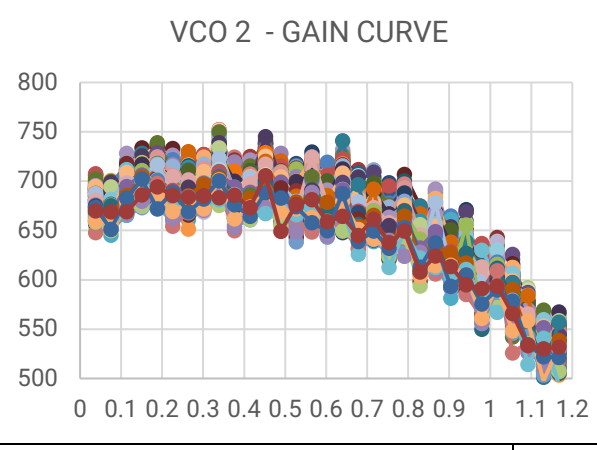

VCO 2
Frequency (MHz)
9800
9600
9400
9200
9000
8800
8600
8400
8200
8000
7800
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
1.1
1.2
vtune (V)

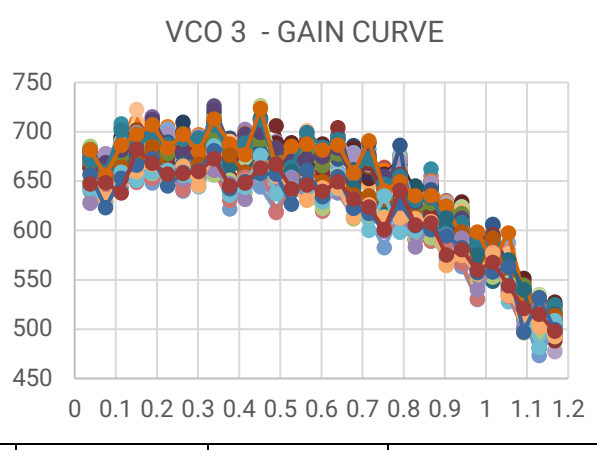

VCO 3
Frequency (MHz)
11000
10800
10600
10400
10200
10000
9800
9600
9400
9200
9000
8800
8600
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
1.1
1.2
vtune (V)

VCO tuning sensitivity - K_{VCO} (MHz/V)









VCO pushing		0.34		1.20	MHz/V
VCO temperature sensitivity		365	100	840	KHz/°C
VCO number of Bands			128		
Input reference			178		MHz
Loop Filter of CPLL			350		KHz
MASH order					programmable
SSB Phase noise measured @ 10GHz	@10KHz		-79.1		dBc/Hz
	@100KHz		-84.7		dBc/Hz
	@1MHz		-110.1		dBc/Hz
	@10MHz		-140.2		dBc/Hz
Charge Pump Programmable Current		0.6		1.4	mA

6.3 Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Characteristics						
LO10G	Single ended output power	RF signal @ 10GHz on 50Ohms	5.22		6.7	dBm
LO20G	Single ended output power	RF signal @ 20GHz on 50Ohms	-1.2		6.61	dBm
Test Digital Output	Digital logic		1.6	1.8	2	V
Input Signal Path						
Reference Input frequency		LVDS/XTAL/TCXO	20		200	MHz
Cascaded RPLL – CPLL characteristics with 40 MHz Crystal Oscillator						

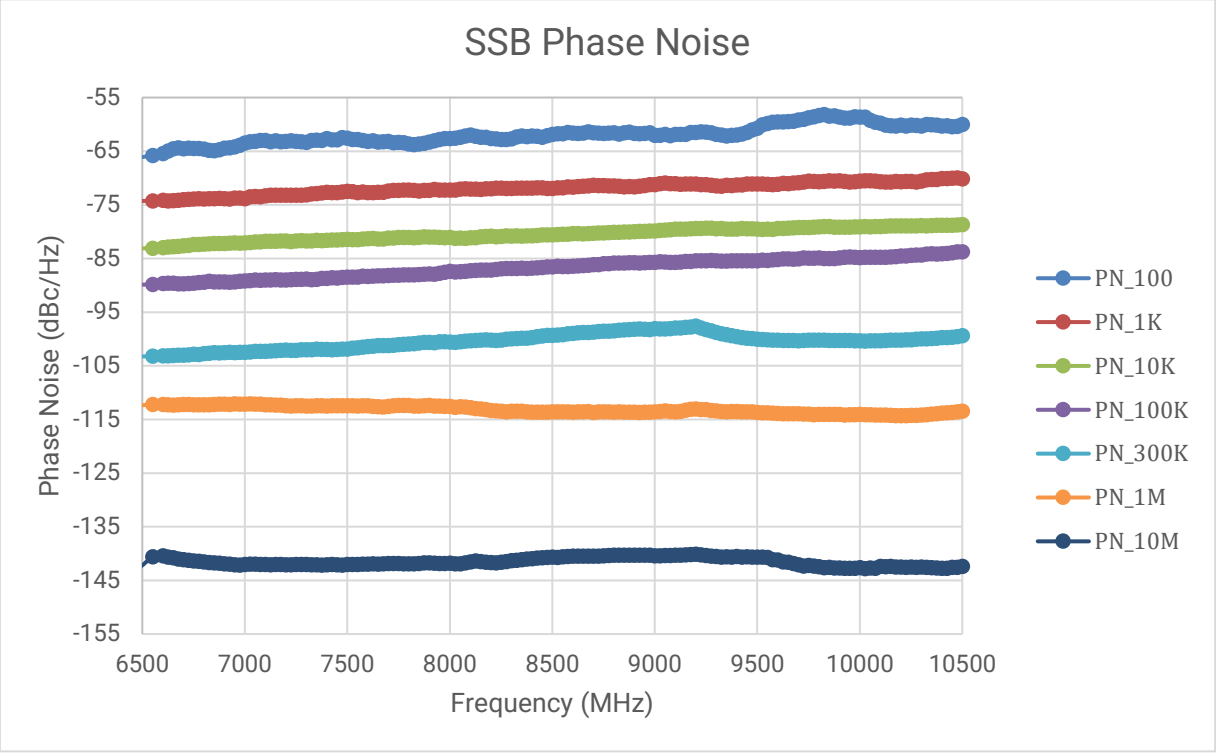


Figure 2. Cumulative phase noise performance of the cascaded PLL measured at 10 GHz path

Chirp Modulation Characteristics					
T_{STL}	Time from chirp triggering to linear slope	1		2	us
T_{CHRP}	Chirp duration	2	25	20000	us
T_{BRKHI}	Constant frequency duration after ramp-up	0		16383	us
T_{FLBK}	Chirp HI to chirp LO duration	0.1		3	us
T_{BRKLO}	Constant frequency duration after flyback	0		16383	us
INL	Frequency error INL (chirp non-linearity, relative to chirp BW)		0.3	1	%
	Data Slope	0.0075	20	60	MHz/us
	Data Slope granularity	0.0075			MHz/us
	Continuous modulation BW (Fstart to Fstop)	1100	1400		MHz

[3] Operating RPLL@100MHz and CPLL@178MHz

6.4 Chirp Characteristics

PARAMETER		Test Conditions							UNIT
Chirp Profile No		***1***	***2***	***3***	***4***	***5***	***6***	***7***	
Chirp profiles	*Center Freq.*	*19.5*	*19.5*	*19.5*	*19.5*	*19.4*	*19.5*	*19.4*	*GHz*
	BW	*550*	*100*	*550*	*200*	*120*	*120*	*120*	*MHz*
	Chirp Time	*40*	*20*	*80*	*40*	*5*	*5*	*10*	*µs*
	Retrace Time	*5*	*0.3*	*10*	*0.3*	*1*	*0.1*	*10*	*µs*
Chirp Begin		14	9	21	10	1.5	1.5	11	µs
Chirp Length Meas.		36	16	70	34	4	4	8.5	µs
Chirp Rate		13.75	4.99	6.88	5	23.79	24.91	-11.99	MHz/ µs
Retrace Chirp Rate		-108.79	-339.43	-55.41	-691.17	-126.75	-837.81	12.03	MHz/ µs
Average Frequency		11.92	2.83	-0.94	2.82	9.75	9.04	4.28	MHz
Meas. Bandwidth		494.97	79.98	481.23	169.99	95.17	99.65	101.90	MHz
Freq. Dev Peak		172.80	223.51	99.61	85.31	1921.57	7894.32	334.72	KHz
Freq. Dev RMS		31.80	35.03	26.99	22.36	425.94	2002.90	52.94	KHz
Freq. Dev AVG		3.98	7.92	-0.153	2.448	-53.36	-654.15	-3.38	KHz
Freq. INL Peak		3.49e-4	2.79e-3	2.07e-4	5.02e-4	2.02e-2	7.92e-2	3.29e-3	
Freq. INL RMS		6.42e-5	4.38e-4	5.61e-5	1.32e-4	4.48e-3	2.01e-2	5.20e-4	
Freq. INL Avg		8.04e-6	9.89e-5	-3.18e-7	1.44e-5	-5.61e-4	-6.57e-3	-3.31e-5	
Min Power		-0.27	-0.03	-0.15	-0.03	1.25	1.26	1.29	dBm
Max Power		1.79	1.05	1.86	1.63	1.85	1.90	1.83	dBm
Power Ripple		2.06	1.08	2.01	1.65	0.59	0.64	0.54	dB
Chirp Profile No		***8***		***9***	***10***	***11***	***12***	***13***	
Chirp profiles	*Center Freq.*	*19.5*		*19.5*	*19.5*	*19.5*	*19.5*	*19.5*	*GHz*
	BW	*300*		*540*	*750*	*300*	*540*	*750*	*MHz*
	Chirp Time	*30*		*45*	*50*	*30*	*45*	*50*	*µs*
	Retrace Time	*8*		*10*	*12*	*1*	*1*	*1*	*µs*
Chirp Begin		15		17	19	8	9	9.5	µs
Chirp Length Meas.		27		42	47	25	40	46	µs
Chirp Rate		10		12	15	10	12	15	MHz/ µs
Retrace Chirp Rate		-37.22		-54.05	-62.70	-314.81	-551.96	-782.91	MHz/ µs
Average Frequency		2.66		3.20	4.00	-7.33	3.20	19.0	MHz
Meas. Bandwidth		269.98		503.97	704.95	249.93	479.97	689.95	MHz
Freq. Dev Peak		199.21		199.19	215.53	538.89	282.17	288.02	KHz
Freq. Dev RMS		35.17		33.34	38.76	74.43	43.32	48.67	KHz
Freq. Dev AVG		7.87		5.83	5.57	17.52	7.21	7.18	KHz
Freq. INL Peak		7.38e-4		3.95e-4	3.06e-4	2.16e-3	5.88e-4	4.18e-4	
Freq. INL RMS		1.30e-4		6.62e-5	5.50e-5	2.98e-4	9.02e-5	7.05e-5	
Freq. INL Avg		2.92e-5		1.16e-5	7.89e-6	7.01e-5	1.50e-5	1.04e-5	
Min Power		-0.07		-0.09	-0.09	-0.01	-0.09	-0.18	dBm
Max Power		1.88		1.86	1.86	1.81	1.85	1.90	dBm
Power Ripple		1.95		1.95	1.95	1.82	1.95	2.08	dB

7 Chirp Generator

The synthesizer can be a part of a multi-chip design, where all chips run on the same digital clock, received from an external source – so that the whole system is completely synchronous. The system transmits and receives a “Frame”, a pre-configured sequence of chirps, which the HW can transmit and receive, without any real-time SW intervention. The SW first configures all the TX and RX chips with the desired relative time offsets, then triggers the frame transmission & processing using only one signal called “SYNC”.

The chirp generator is a predefined time engine that controls the MASH operation and delivers an automated predefined waveform for the chirp generation of the Chirping PLL. This waveform is initiated by either the pin (SYNC) or via an SPI trigger command. During that time the chirper remains in BUSY state until the whole waveform is played.

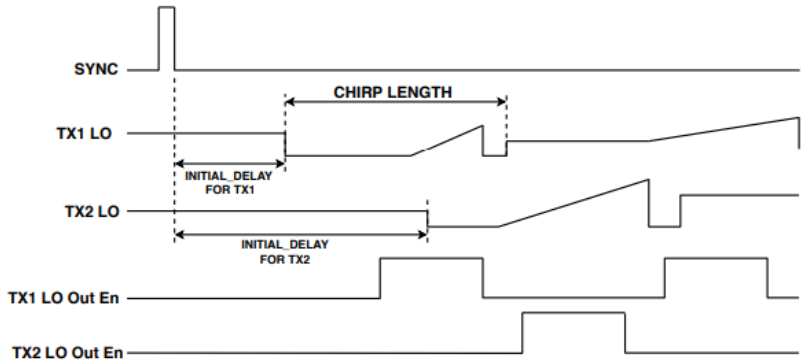


Figure 3. Frame Transmission

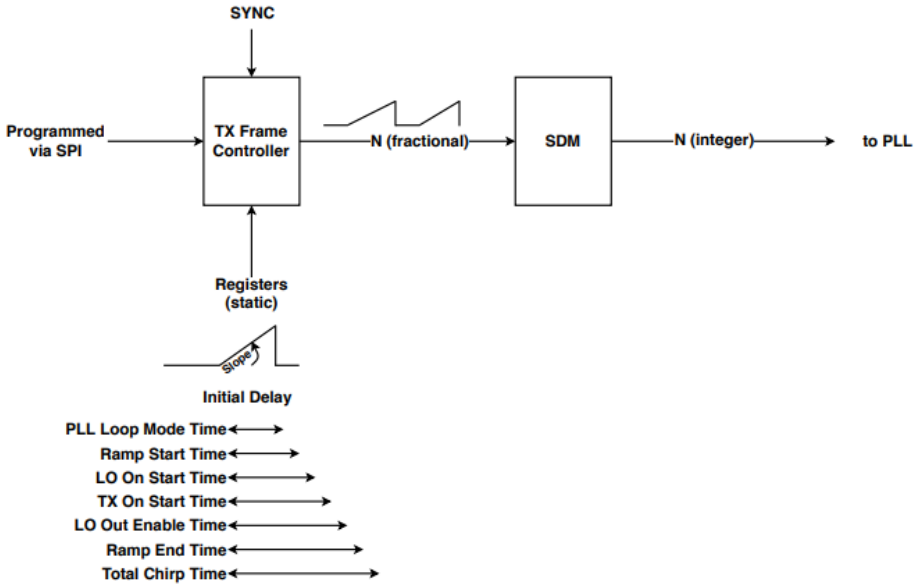


Figure 4. Tx Registers

As shown below in yellow, there is the Leading Segment of a constant frequency with a fixed delay followed by the Frame that is a complex waveform. One **Frame** consists of various **Periods**, The Period is identical waveform that are played over and over again from 1 up to 4095 times, or even infinitely if programmed accordingly.

Subdivisions of the Period are the **Clusters**, ranging from 1 up to 28. Each cluster draws data from one of the 28 **Profiles Registers** and can be replayed up to 4096 times before proceed to the next profile. A Cluster can be totally skipped by setting 0 to the corresponding number of repetitions.

The **Profile Registers** data consist by :

- 3 Frequencies (low, high, final),
- 2 slops (up, down),
- 4 durations (up, high, down, low),
- leaker sign (0,+,-), and
- the PEF Gain for each frequency.

Furthermore, each Profile includes definitions (Start-of- / End-of-) of the power detection and linear segments (flags)

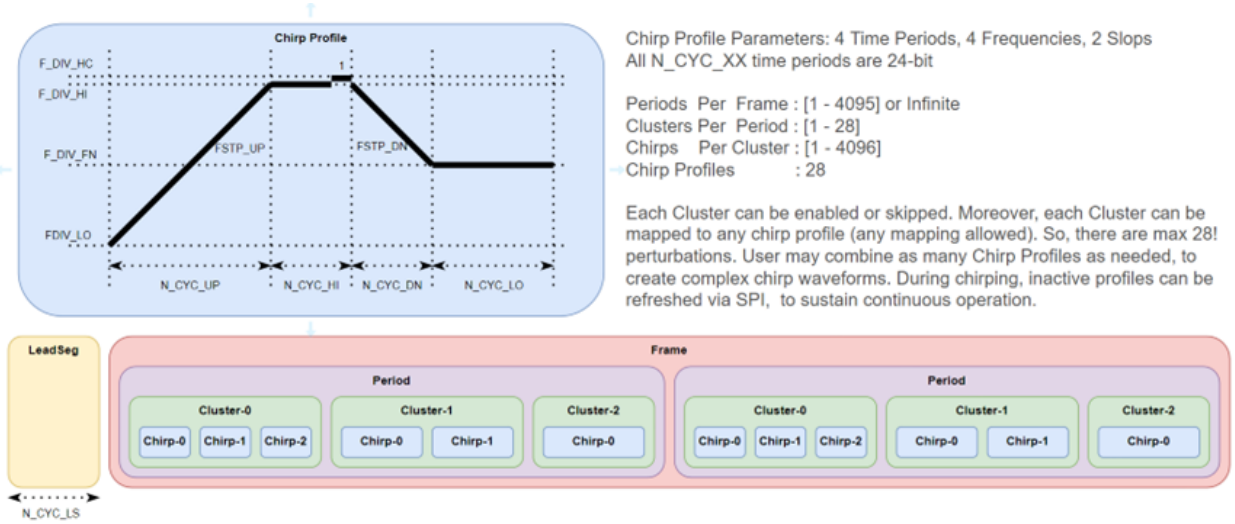


Figure 5. Frame – Period – Clulster - Chirp ordering

7. 1 Chirp profiles and INL

Please contact Weasic for this information.

7.2 Controller

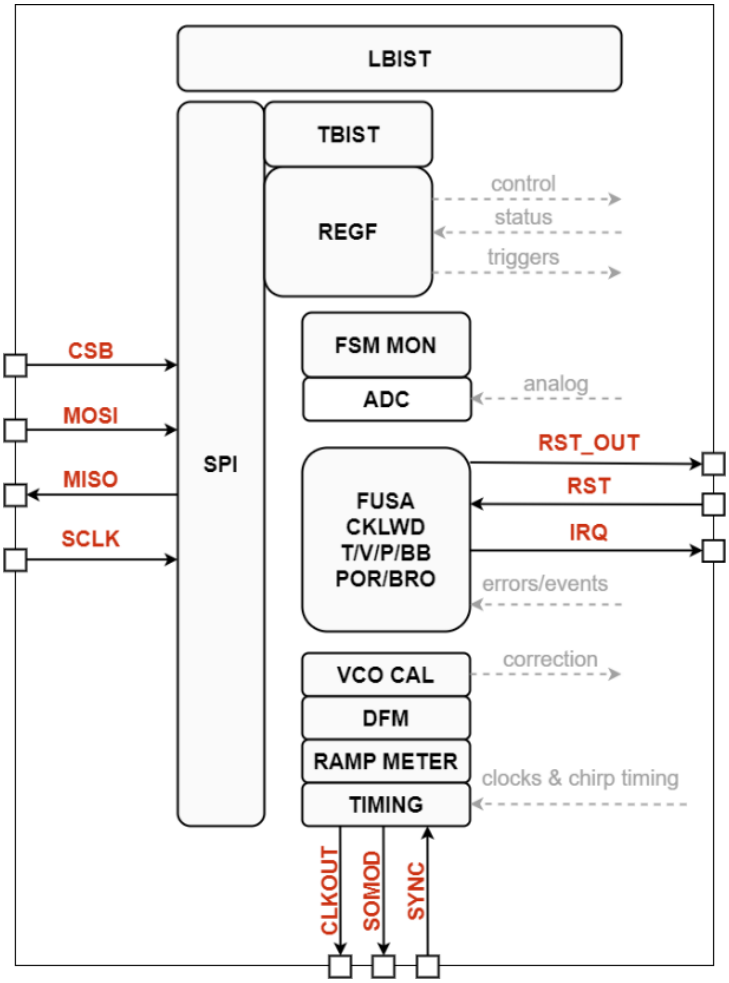


Figure 31. Functional Block Diagram of the Controller

- SPI: SPI Interface, for Control & Status by the system Host
- REGF: SPI Register File, stores chip configuration
- TBIST: Transparent BIST of Reg file contents, checks for SEUs (Single-Event-Upsets). Periodically triggered by a timer, verifies the CRC of the REGF registers, serially bit by bit.
- LBIST: Logic BIST of the whole chip. Checks for stuck-at faults, by applying test vectors into the scan chains.
- FUSA: Functional Safety Features.
- T/V/P/BB: Temperature / Voltage / Power / Ball-Breaks Detectors (over/under)

  - ➢ Temperature sensor: Absolute accuracy: +/- 6.73 ºC @ 125 ºC (uncalibrated) / +/- 1.5 ºC @ 125 ºC (calibrated)
  - ➢ Brown Out detector with Fixed 10% Under Voltage Sensor
- POR/BRO: Power-On-Reset, Brown-Out-Detector.
- CLKWD: Clock Watchdog, issues an error flag when clock stops toggling.
- FSM_MON: Continuous Monitor, periodically triggered by a timer, measures sensors by the ADC and issues error flags when out of certain thresholds.
- VCO_CAL: Auto-Calibration algorithms of the chip VCOs. Tune VCO capacitors and eliminate frequency drift due to manufacturing process variations
- DFM: Digital Frequency Meter. Measures the clock frequency of the one clock, using the other clock as reference.
- RAMP_METER: Measures the Ramp Frequency during chirping and issues error flags when out of certain thresholds.

The table that shows the functionality of all the analog test points is shown below:

ATB Control	description	BIAS POINT	Estimated Voltage (V)
0	RPLL	LDO1V2 Charge Pump supply	1.1-1.3
1	RPLL	LDO0V8 PFD-CP drivers	0.7-0.88
2	RPLL	LDO0V8 PRESCALER-MASH - LOGIC	0.7-0.88
3	RPLL	LDO0V8 - CLKGEN	0.7-0.88
4	RPLL	Reference of LDO0V8 (Digital)	0.8
5	RPLL	Reference of LDO Charge Pump	1.2
6	RPLL	Charge Pump Pmos reference	1.2-0.9
7	RPLL	Charge Pump Nmos reference	0- 0.3
8	RPLL	VDD RPLL Supply 1V8 X 0.5	0.9
9	RPLL	Supply 1V8 X 0.5	0.9
10	RPLL	Charge Pump output	0 - 1.2
11	RPLL	Charge Pump Dummy output	0 - 1.2
12	RPLL	VCO Common Drain Voltage	0.2 - 0.3
13	RPLL	VCO Common Gate voltage	0.4 - 0.7
14	RPLL	LDO VCO output	1.2
15	RPLL	LDO VCO Buffer output	1.2
16	RPLL	VCO Vtune	0 - 1.2
17	RPLL	VCO1V8 Supply X 0.5	0.9

18	LOPATH	buff10G Gate	0.226
19	LOPATH	Doubler Source	0.112
20	LOPATH	Doubler Gate	0.112
21	LOPATH	buf20G Gate	0.29
22	LOPATH	PA20G Drain	0.55
23	LOPATH	PA20G Gate	0.243
24	LOPATH	PA20G VDD1V8	0.9
25	LOPATH	PA20G VSS	0.001
26	LOPATH	VSS	0
27	LOPATH	vPowerSense	0.041
28	LOPATH	VDDLDO0V8	0.82
29	LOPATH	buffPA10G Gate	0.27
30	LOPATH	PA10G Drain	0.495
31	LOPATH	PA10G Gate	0.284
32	LOPATH	PA10G VDD1V8	0.9
33	LOPATH	PA10G VSS	0
34	LOPATH	PA5G Drain	0.48
35	LOPATH	PA5G Gate	0.304
36	LOPATH	PA8G VDD1V8	0.9
37	LOPATH	PA9G VSS	0
38	LOPATH	buffPA5G Gate	0.27
39	LOPATH	divider Gate	0.241
40	LOPATH	VSS	0
41	LOPATH	VSS	0
42	LOPATH	VSS	0
43	LOPATH	LDO reference	0.82
44	LOPATH	VDD1V8	0.9
45	LOPATH	VBGR	1.231
46	LOPATH	VSS	0
47	LOPATH	VSS	0
48	CPLL	Loop Filter Charge Pump output	0.6
49	CPLL	Loop Filter RZ-CZ node	0 -1.2
50	CPLL	Loop Filter Active Loop opamp output	0 - 1.2
51	CPLL	Loop Filter Vtune input	0 - 1.2
52	CPLL	LDO0V8 PFD-CP drivers	0.8
53	CPLL	LDO0V8 PRESCALER-MASH - LOGIC	0.8
54	CPLL	LDO0V8 - CLKGEN Prescaler RaMet	0.8
55	CPLL	LDO0V8 - Prescaler Calibration	0.8

56	CPLL	Reference of LDO Charge Pump	1.2
57	CPLL	Reference of LDO0V8 (Digital)	0.8
58	CPLL	Charge Pump Pmos reference	1.2-0.9
59	CPLL	Charge Pump Nmos reference	0- 0.3
60	CPLL	RCMON-V1500	1.5
61	CPLL	RCMON-V1200	1.2
62	CPLL	RCMON-V0900	0.9
63	CPLL	RCMON ramp	0 -1.5
64	CPLL	VDDCP 1.8V X 0.5	0.9
65	CPLL	VDDPLL 1.8V X 0.5	0.9
66	CPLL	LDO 1.2V OUTPUT	1.2
67	CPLL	CP Active Loop reference	0.6 / 1.2
68	CPLL	VDD RPLL Supply 1V8 X 0.5	0.9
69	CPLL	VTUNE of CPLL	0.1 - 1.2
70	CPLL	LDO output	1.23
71	CPLL	VCO0 output	1.23
72	CPLL	VCO1 output	1.23
73	CPLL	VCO2 output	1.23
74	CPLL	VCO3 output	1.23
75	CPLL	VCO0 pmos gate bias	0.7
76	CPLL	VCO1 pmos gate bias	0.7
77	CPLL	VCO2 pmos gate bias	0.7
78	CPLL	VCO3 pmos gate bias	0.7
79	CPLL	No USE	0
80	CPLL	No USE	0
81	CPLL	No USE	0
82	CPLL	No USE	0
83	CPLL	No USE	0
84	BIAS	Calibrated Voltage	0.2-0.6
85	BIAS	Exteres Voltage	0.45
86	BIAS	BGR Voltage	1.2
87	BIAS	Buffered Voltage	1.2
88	ADC	ADC digital Supply	0.8
89	ADC	ADC Ground	0
90	ADC	ADC INP	0 - 1.5
91	ADC	ADC INN	0.4 -0.9
92	TEMP	TEMP SENSOR OUTPUT	0 -1.5
93	BIAS	No USE	No USE
94	BIAS	No USE	No USE
95	BIAS	No USE	No USE
96	PADRING	BGR LDO 0.8V	1.2

97	PADRING	Digital LDO reference	0.86
98	PADRING	VDDCORE DIGITAL	0.86
99	PADRING	PWM signal	0 -0.9

8 Layout

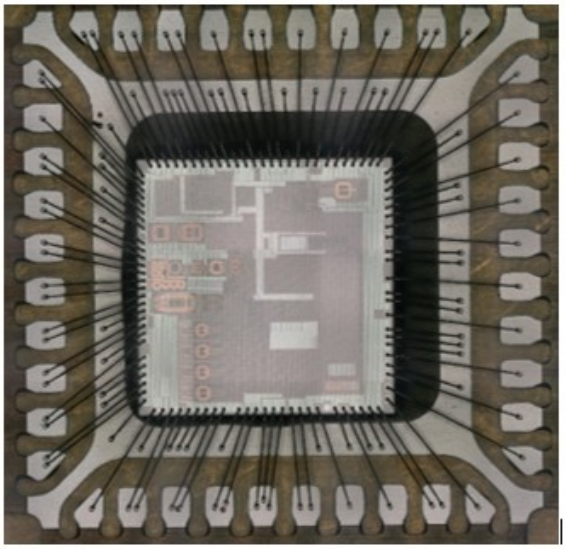


Figure 6. Layout area of the Frequency Synthesizer

9. Evaluation Board

Figure 7. EVB is available upon request

About weasic

Weasic Microelectronics S.A. designs, develops, and markets high quality complex analog and RF IP for wireless communications and wireless sensors applications, helping semiconductor and system companies to shrink the product design cycle. WEASIC, silicon verified IP is designed in the state of the art CMOS, CMOS-SOI and SiGe processes and can be easily ported and customized to serve the development of 5G and Backhaul communications transceivers, mmWave front-end modules, and RADAR sensors.

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