24.10

sensor to image

a Euresys Company

sensor to image

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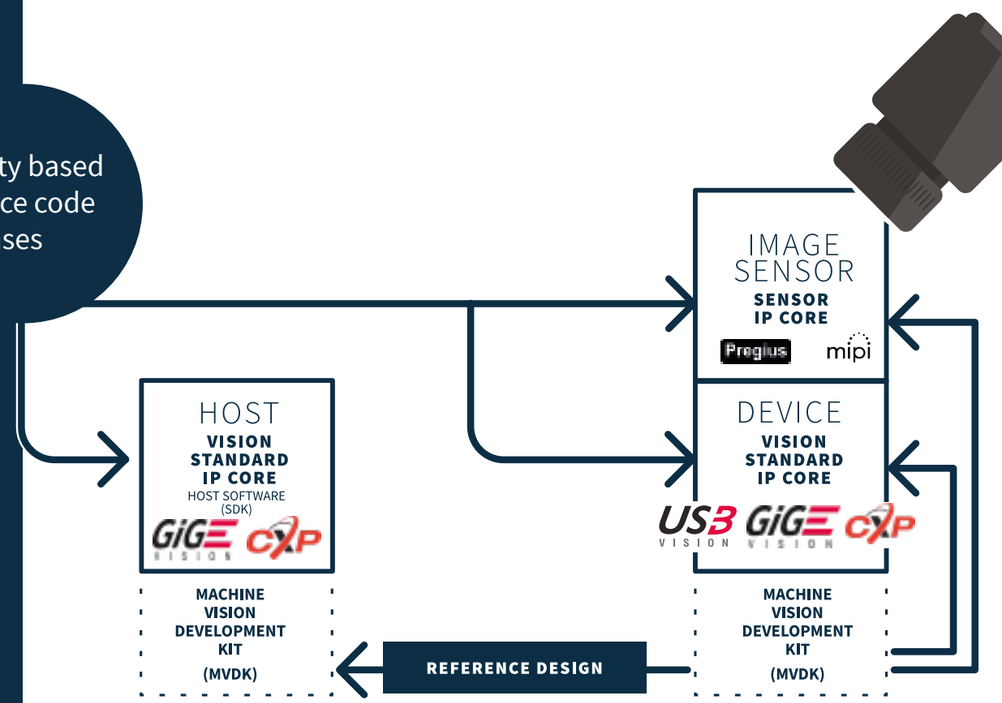
Quantity based or source code IP licenses



IP Core Concept

IP Cores are widely used in FPGA development to incorporate proven functionality in a design. They reduce development time and increase design quality, especially in complex designs.

The IP Cores from Sensor to Image for the GigE Vision, USB3 Vision and CoaXPress transport layers and the SubLVDS and MIPI-CSI2 sensor interfaces are designed to support customers in building their own vision components.

A typical device design consists of several functional blocks as well as IP Cores from the FPGA vendor. The architecture may be complex, requiring from the developer a good knowledge of the FPGA and firmware.

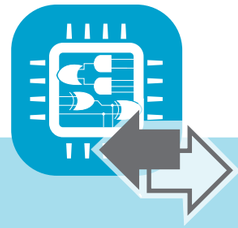
To facilitate the integration of Sensor to Image's IP Cores, it is our philosophy to provide a fully functioning reference design for an evaluation platform as similar as possible to the target platform. These reference designs help speed up integration and reduce development costs.

MVDK

MACHINE VISION DEVELOPMENT KIT

AT A GLANCE

- All major machine vision interfaces available on a single development board
- GigE Vision, CoaXPress and USB3 Vision compliant platform
- Sony IMX Pregius and MIPI CSI-2 evaluation platform
- GigE Vision up to 10 Gbps, CoaXPress up to CXP-12
- Support for Enclustra Mercury FPGA modules with AMD FPGAs

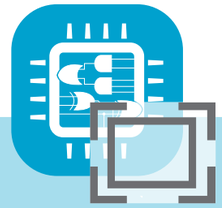


Vision Standard IP Cores

GIGE VISION, USB3 VISION, COAXPRESS

AT A GLANCE

- Compatible with AMD, Altera and Microchip Polarfire FPGAs
- Compact, customizable
- Delivered as working reference design



Sensor IP Cores

IP CORES FOR SONY PREGIUS SUB-LVDS AND MIPI CSI-2 IMAGE SENSORS

AT A GLANCE

- Image sensor data deserialization and decoding
- Software library for sensor configuration
- Compatible with AMD FPGAs
- Delivered as working reference design for fast development

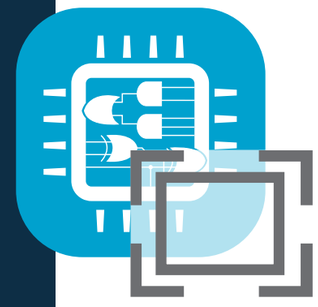
Vision Standard Software

USB3 & GIGE VISION

AT A GLANCE

- Host Software SDK for GigE Vision and USB3 Vision
- GigE Vision Camera simulator
- Compatible with Windows and Linux
- Available as source code

Flexible IP Cores Licensing Models



Sensor to Image grants licenses to use Intellectual Property (IP).
Depending on the use case, there are different licensing models available. Licensing is typically done as a “Project License”, that means

- One FPGA family,
- A dedicated design team,
- Changing FPGA family requires a “project upgrade”,
- Multi-project Licensing is possible at higher price and some support constraints.

Depending on the production volume and design complexity, a licensing model may be offered for:

- a Single Piece license, including an encrypted VHDL IP Core. This licensing model presents the lowest up-front cost, but has a recurring cost of the license chips which are purchased from S2I directly. This model is the “Starter Edition” and suitable for a design very similar to a standard reference design and low production quantity. Not all features of an IP are supported in this model.
- a Volume license, including more support, reduced cost for license chips (if required) and sometimes VHDL source code. Volume and upgrade discounts are available. This model is the “Professional Edition” and is suitable for complex designs or higher production quantities.

Optional maintenance contracts ensure staying up to date with the IP and getting long term support.

Machine Vision Standards

Technology Standards help simplify the market and reduce complexity for specific technologies. In the machine vision industry, standards help to compare products from different vendors, enable interoperability and gain wide market acceptance.

Over the last 20 years, the industry has developed and maintained several new digital standards to address the growing spectrum of use cases.

Transport layer standards provide access to the camera's registers and define data streams for images or other data.

The most important transport layer standards for which Sensor to Image proposes IP Cores are:

GigE Vision

GigE Vision is a global camera interface standard developed using the Gigabit Ethernet communication protocol. GigE Vision allows for fast image transfer using low-cost standard cables over very long lengths. With GigE Vision, hardware and software from different vendors can interoperate seamlessly over GigE connections.

GigE Vision is a widely adopted interface around the world, with dozens of leading companies currently offering hundreds of GigE Vision compliant products. GigE Vision offers many benefits including:

- **FAST**: High bandwidth (115 MiB/s@1Gbps, 1150MiB/s@10Gbps) transfers large images quickly in real time
- **ABUNDANT:** Uncompromised data transfer up to 100 meters in length over copper or even longer over fiber
- **STANDARD:** Low cost CAT5e or CAT6 cables and standard connectors
- **SCALABLE:** Highly scalable to the fast growth of Ethernet
- **LOW COST:** Standard hardware and cables allow easy, low cost integration

USB3 Vision

The USB3 Vision® interface is based on the standard USB 3.x interface found on all current PCs and many embedded systems. Cameras and other devices utilizing this standard are compatible with a wide range of products from many vendors.

- High bandwidth and low-performance overhead
- Easy-to-use plug and play interface
- Power and data over the same passive cable up to five meters (more with active cables)

CoaXPress

The CoaXPress digital interface was developed for high-speed image data transmission and intended mainly for machine vision applications. The interface is also suitable for other imaging applications and for high-speed data transmission in other fields. CoaXPress uses coaxial cables as a physical medium, and recently also supports optical cables.

CoaXPress is hosted by the Japan Industrial Imaging Association (JIIA). The JIIA CoaXPress Technical Committee is responsible for the preparation and maintenance of the standard. Contributions are also made by the CoaXPress Consortium and the CoaXPress Liaison Group, which is for members of the A3 and EMVA.

CoaXPress-over-Fiber

The CoaXPress-over-Fiber concept is based on Ethernet physical medium topologyand on a series of rules to map the CoaXPress protocol to the interface of the Ethernet physical layer. Based on these rules, a CoaXPress to Ethernet Physical Layer bridge (CXP-PHY bridge) is specified to allow the CoaXPress protocol to be transported over available existing Ethernet components without the need to establish new fiber components for the CoaXPress standard.

(Source : automate.org & jiia.org)

GenICam

GenICam is a global set of standards to interface industrial cameras to computer software applications (such as machine vision). It allows a homogenization of the wording, the interfaces and the processes in image processing, acquisition and transport. By providing all users with a common set of names and configurations, it ensures communication regardless of the supplier implementation details, feature set, or interface technology. It is the basis for video standards like GigE Vision, USB3 Vision, CoaXPress or Camera Link.

Sensor to Image provides developers with products to make device and software development easier. For this we offer a wide range of FPGA IP Cores and software development kits, listed on the following pages.

GigE Vision **Device** IP Core

GigE Vision Device IP Core for FPGA

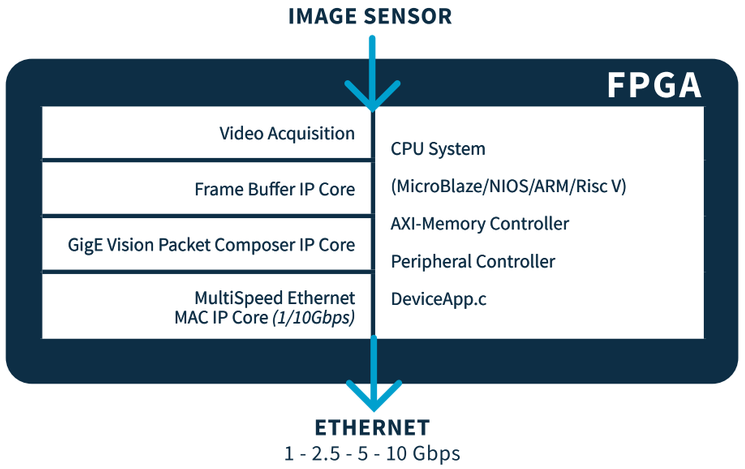
AT A GLANCE

- Compatible with AMD 7 Series (and newer) and Altera Cyclone V devices (and newer)
- Preliminary compatibility with Microchip PolarFire
- Compact, customizable
- Speed support from 1 Gbps to more than 10 Gbps
- Delivered as working reference design

GigE Vision IP Core Description

GigE Vision is a standard communication protocol for vision applications based on the well-known Ethernet technology. It allows easy interfacing between GigE Vision devices and PCs running TCP/IP protocol family. Sensor to Image offers a set of IP cores and a development framework to build FPGA-based transmitter products using the GigE Vision interface. Due to the speed of GigE Vision, especially at speeds higher than 1 Gbps, senders require a fast FPGA-based implementation of the embedded GigE core. The GigE Vision core set is compatible with AMD 7 Series devices (and newer), Altera Cyclone V devices (and newer) and Microchip PolarFire.

This IP supports GigEVision 1.x and 2.x.



RESOURCE USAGE

https://www2.euresys.com/S2i-GigEVision-Device-IP-Core

GigE Vision **Host** IP Core

GigE Vision Host IP Core for FPGA

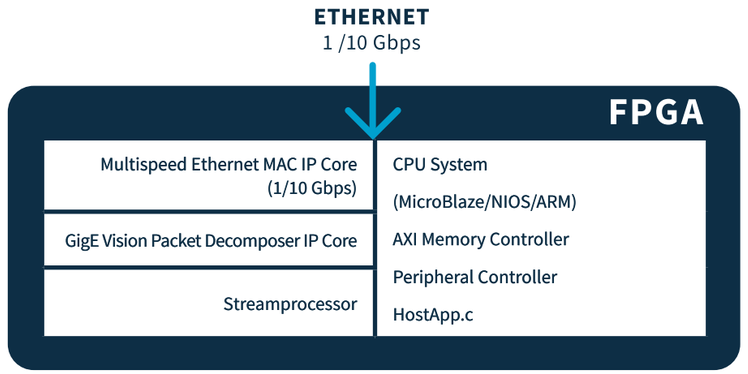
AT A GLANCE

- Compatible with AMD 7 Series (and newer), Altera Cyclone V devices (and newer)
- Compact, customizable
- Speed support from 1 Gbps to more than 10 Gbps
- Delivered as working reference design

GigE Vision® Host IP Core Description

GigE Vision is a standard communication protocol for vision applications based on the well-known Ethernet technology. It allows easy interfacing between GigE Vision devices and PCs running TCP/IP protocol family. Sensor to Image offers a set of IP cores and a development framework to build FPGA-based receiver products using the GigE Vision interface. Due to the speed of GigE Vision, especially at speeds higher than 1 Gbps, receivers require a fast FPGA based implementation of the embedded GigE core. The GigE Vision core set is compatible with AMD and Altera devices.

This IP supports GigEVision 1.x and 2.x.



RESOURCE USAGE

https://www2.euresys.com/S2i-GigEVision-Host-IP-Core

GigE Vision Host Software

Software Development Kit for GigE Vision compliant applications

AT A GLANCE

- GigE Vision and GenICam compatible SDK
- Compatible with Windows and Linux operating system
- X86 and ARM32/64 support
- Source Code available

Sphinx GigE Vision Transport Layer SDK Description

Sensor to Image provides a feature-rich software toolkit that provides the building blocks required to quickly and easily design high-performance image acquisition applications.

This software kit consists of several components:

The Sphinx GigE Vision Viewer is a desktop application to discover and configure GigE Vision compliant cameras. It also receives GigE Vision streams and displays them.

A transport layer library (Sphinx GigE Vision Library) implements all lower level transport layer specific tasks and provides either an intuitive proprietary API or acts as GenTL producer with the GenTL compliant interface.

For performance optimization a Filter driver is provided to reduce CPU load and increase system stability.

The Sphinx GigE Vision SDK supports all mandatory and most of the optional features defined by the GigE Vision specification up to version 2.2. Both Windows and Linux operating systems are supported.

Depending on the license, the components of the SDK are partially or completely delivered as C source code.

https://www2.euresys.com/S2i-GigEVision-Host-Software

GigE Vision Server

Software based GigE Vision Device Implementation

AT A GLANCE

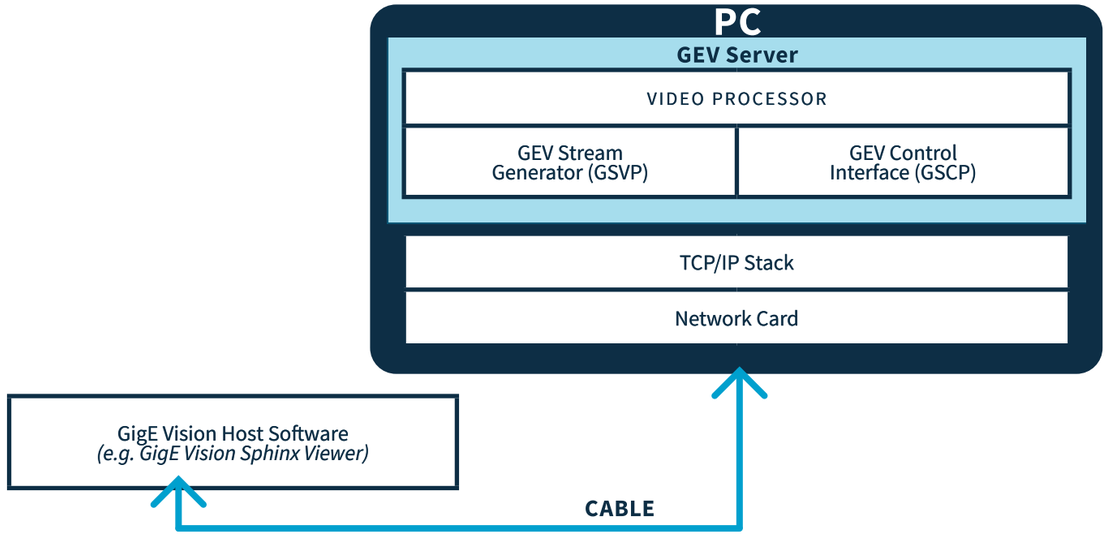
- GigE Vision and GenICam compatible SDK to emulate GigE Vision transmitters
- Compatible with Windows and Linux operating system
- X86 and ARM32/64 support
- Full source code delivery

Sphinx GigE Vision SERVER Description

The GigE Vision Server software package is for creating software-based GigE Vision device applications.

This is useful for software based GigE Vision emulation or CPU based devices, that do not have high data rate requirements (for those applications refer to the FPGA IP Core) or for prototyping of GigE Vision devices.

With the package, it is possible to design GigE Vision 1.x or 2.x compliant devices for Windows or Linux operating systems. As the server is delivered in full C-source code, it can be extended with specific features.



https://www2.euresys.com/S2i-GigEVision-Server

CoaXPress **Device** IP Core

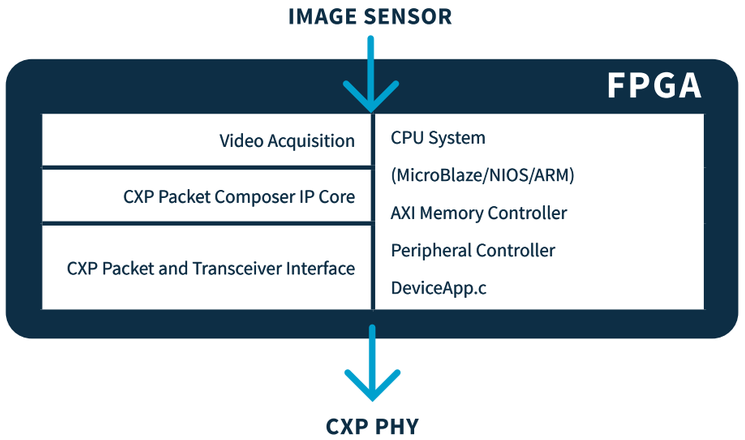
CoaXPress Device IP Core for FPGA

AT A GLANCE

- Compatible with AMD 7 Series (and newer), Altera Cyclone 10 devices (and newer)
- Preliminary compatibility with Microchip PolarFire
- Compact, customizable
- Speed support from 1 Gbps to more than 50 Gbps
- Delivered with a working reference design

CoaXPress IP Core Description

CoaXPress (CXP) is a standard communication protocol for vision applications based on widely used coaxial cables. It allows easy interfacing between cameras and frame grabbers and supports the GenICam software standard. Sensor to Image offers a set of IP Cores and a development framework to build FPGA-based transmitters using the CoaXPress interface. Due to the speed of CXP, senders require a fast FPGA-based implementation of the CXP core, using embedded transceivers. CXP cores are compatible with AMD 7 series devices (and newer), Altera Cyclone 10 devices (and newer) and Microchip PolarFire Series.



RESOURCE USAGE

https://www2.euresys.com/S2i-CoaXPress-Device-IP-Core

CoaXPress **Host** IP Core

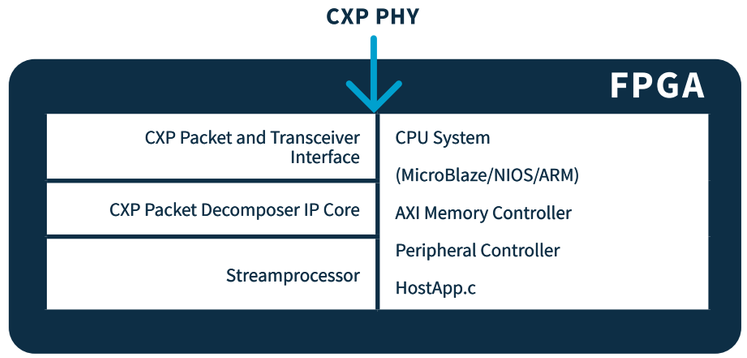
CoaXPress Host IP Core for FPGA

AT A GLANCE

- Compatible with AMD 7 Series (and newer), Altera Cyclone 10 devices (and newer)
- Compact, customizable
- Speed support from 1 Gbps to more than 50 Gbps
- Delivered as working reference design

CoaXPress Host IP Core Description

CoaXPress (CXP) is a standard communication protocol for vision applications based on widely used coaxial cables. It allows easy interfacing between cameras and frame grabbers or embedded processors and supports the GenICam software standard. Sensor to Image offers a set of IP cores and a development framework to build FPGA-based receivers using the CoaXPress interface. Due to the speed of CXP, receivers require a fast FPGA-based implementation of the CXP core, using embedded transceivers. The CXP Host core is compatible with AMD and Altera devices.



RESOURCE USAGE

https://www2.euresys.com/S2i-CoaXPress-Host-IP-Core

CoaXPress over-Fiber

CoaXPress over-Fiber **Device** Bridge IP Core

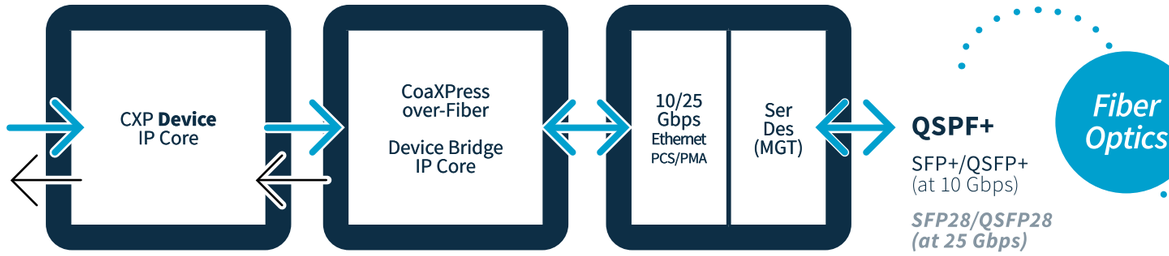
CoaXPress-over-Fiber Device Bridge IP Core for FPGA

AT A GLANCE

- CXP to nGMII Bridge IP Core
- Compatible with AMD 7 Series (and newer), Altera Cyclone 10/Arria 10/Agilex
- Compatible with S2I and third-party CoaXPress Device IP Cores
- Delivered as working reference design (when licensed with the S2I CoaXPress Device IP Core) and extensive simulation testbench

CoaXPress-over-Fiber Bridge IP Core Description

The CoaXPress-over-Fiber Device Bridge IP Core allows to connect a CoaXPress Device IP Core to an nGMII (10/25 Gbps Media Independent Interface) bus inside an FPGA. nGMII, as defined in IEEE Std 802.3 Clause 46, is the main access to the 10/25G Ethernet physical layer. The generic nature of this interface facilitates mapping the CoaXPress signaling into the PCS/PMA Ethernet sublayers. The IP converts CoaXPress control and streaming packets to nGMII packets going towards an Ethernet PCS/PMA block.



What is CoaXPress-over-Fiber ?

CoaXPress-over-Fiber is a light but significant extension of the existing CoaXPress specification to support transport over fiber optics. CoaXPress (CXP) is the de-facto standard for high-bandwidth computer vision applications. CoaXPress 2.1, the latest version of the specification, specifies the CXP-12 speed, a 12.5 Gbps (Gigabit per second) connection over a coaxial copper cable. As link aggregation is common with CoaXPress, bandwidths of 50 Gbps (12.5 x 4) are easily achievable with four CXP-12 connections. CoaXPress-over-Fiber has been designed as an add-on to the CoaXPress specification. It provides a way to run the CoaXPress protocol, as it is, unmodified, over a standard Ethernet connection, including fiber optics. As such, CoaXPress-over-Fiber uses standard electronics, connectors and cables designed for Ethernet, but the protocol is CoaXPress, not Ethernet, not GigE Vision.

RESOURCE USAGE

https://www2.euresys.com/S2i-CXP-over-Fiber-Device-IP-Core

CoaXPress over-Fiber

CoaXPress over-Fiber **Host** Bridge IP Core

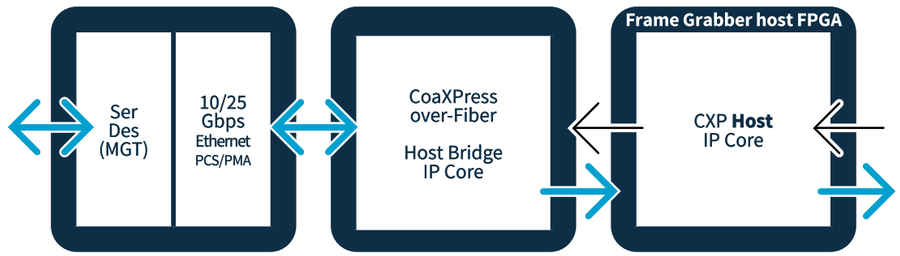
CoaXPress-over-Fiber Host Bridge IP Core for FPGA

AT A GLANCE

- nGMII to CXP Bridge IP Core
- Compatible with AMD 7 Series (and newer), Altera Cyclone/Arria 10/Agilex
- Compatible with S2I and third-party CoaXPress Host IP Cores
- Delivered as working reference design (when licensed with the S2I CoaXPress Host IP Core) and extensive simulation testbench

CoaXPress-over-Fiber Bridge IP Core Description

The CoaXPress-over-Fiber Host Bridge IP Core allows to connect a CoaXPress Host IP Core to an nGMII (10/25 Gbps Media Independent Interface) bus inside an FPGA. nGMII, as defined in IEEE Std 802.3 Clause 46, is the main access to the 10/25G Ethernet physical layer. The generic nature of this interface facilitates mapping the CoaXPress signaling into the PCS/PMA Ethernet sublayers. The IP converts nGMII packets received from an Ethernet PCS/PMA block, back to CoaXPress packets.



What are the benefits of using CoaXPress-over-Fiber for my application?

- Available as CXP to nGMII (device) or nGMII to CXP (host) Bridge IP Cores
- Ultra-high data/frame rates
- Many accessory and cabling options to cover any length requirement
- Low CPU overhead, low latency, low jitter image acquisition
- Highest camera count per PC performance
- Very competitive cost/performance ratio
- Wide industry acceptance due to JIIA standardization
- Ready for CXP25

RESOURCE USAGE

https://www2.euresys.com/S2i-CXP-over-Fiber-Host-IP-Core

USB3 VISION

USB3 Vision Device IP Core

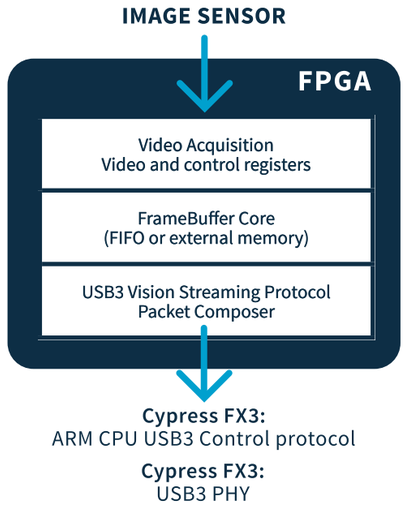
USB3 Vision Device IP Core for FPGA

AT A GLANCE

- Compatible with AMD 7 Series (and newer) and Altera Cyclone V devices (and newer)
- Compact, customizable
- Delivered as working reference design

USB3 Vision IP Core Description

USB3 Vision is a standard communication protocol for vision applications based on the widely used USB 3.0 interface. As the protocol is standard and supports GenICam, it allows easy interfacing between cameras and PCs. Sensor to Image offers a set of IP Cores and a development framework to build FPGA-based products using the USB3 Vision interface. Due to the speed of USB3 Vision, senders and receivers require a fast FPGA-based implementation of the embedded USB core. USB3 Vision IP Cores are compatible with AMD 7 Series devices (and newer) and Altera Cyclone V devices (and newer).



RESOURCE USAGE

https://www2.euresys.com/S2i-USB3Vision-Device-IP-Core

USB3 VISION

USB3 Vision Host Software

Software Development Kit for USB3 Vision compliant applications

AT A GLANCE

- USB3 Vision and GenICam compatible SDK
- Compatible with Windows and Linux operating systems
- Source Code available

Sphinx USB3 Vision Transport Layer SDK Description

Sensor to Image provides a feature-rich software toolkit that provides the building blocks needed to quickly and easily design high-performance image acquisition applications.

This software kit consists of several components:

The Sphinx USB3 Vision Viewer is a desktop application to discover and configure USB3 Vision compliant cameras. It also receives USB3 Vision streams and displays them.

A transport layer library (Sphinx USB3 Vision Library) implements all lower-level transport layer specific tasks and provides either an intuitive proprietary API or acts as a GenTL producer with the GenTL compliant interface.

The software is delivered with a customizable USB3 Vision class driver.

The Sphinx USB3 Vision SDK supports all mandatory and most of the optional features defined by the USB3 Vision specification up to version 1.2. Both Windows and Linux operating systems are supported.

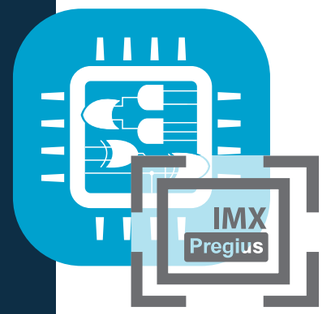
Depending on the license, the components of the SDK are partially or completely delivered as C source code.

https://www2.euresys.com/S2i-USB3Vision-Host-Software

Pregius

IMX Pregius IP Core

IP Core for Sony Pregius Sub-LVDS image sensors

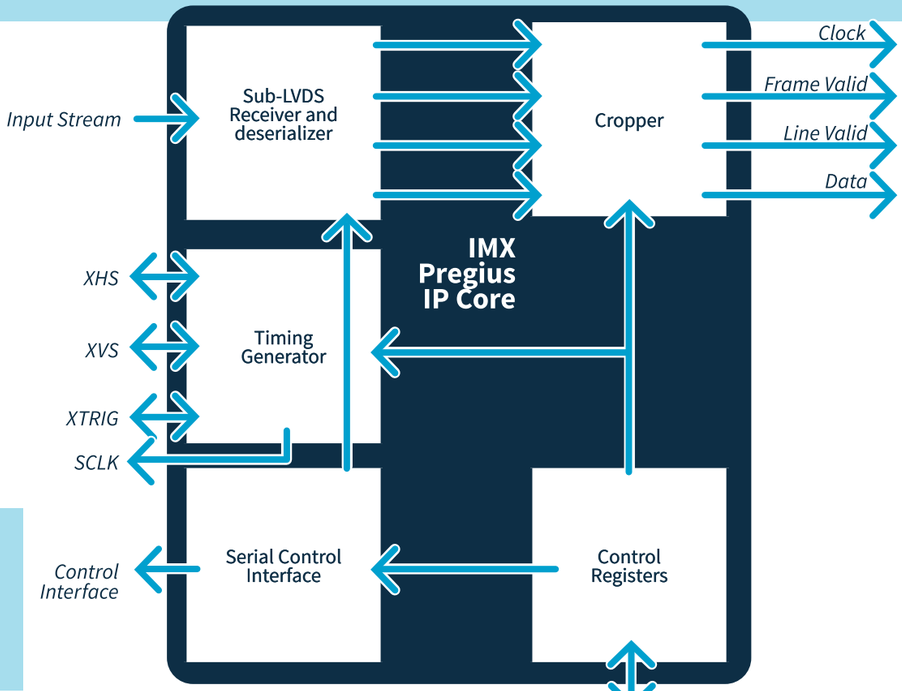


AT A GLANCE

- Sub-LVDS readout and decoding block
- SPI-based sensor configuration module
- Software library for sensor configuration
- Free running or triggered readout modes

IMX Pregius IP Core Description

The IMX Pregius from Sony is a series of widely used, high quality CMOS image sensors. S2I's IMX Pregius IP Core supports these sensors, it is able to read their data as well as controlling them. It is delivered as a fully functioning reference design that is running on an agreed common delivery patform along with an FMC module compatible with S2I's MVDK and standard FPGA evaluation kits. Together, they provide an easy way to design a camera.



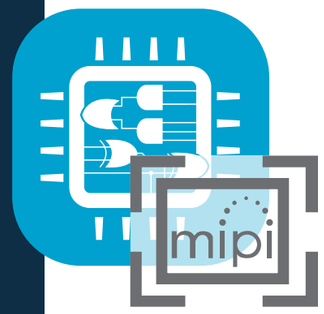
RESOURCE USAGE

https://www2.euresys.com/S2i-IMX-Pregius-IP-Core

mipi

MIPI CSI-2 Receiver IP Core

IP Core for MIPI CSI-2 Imagers

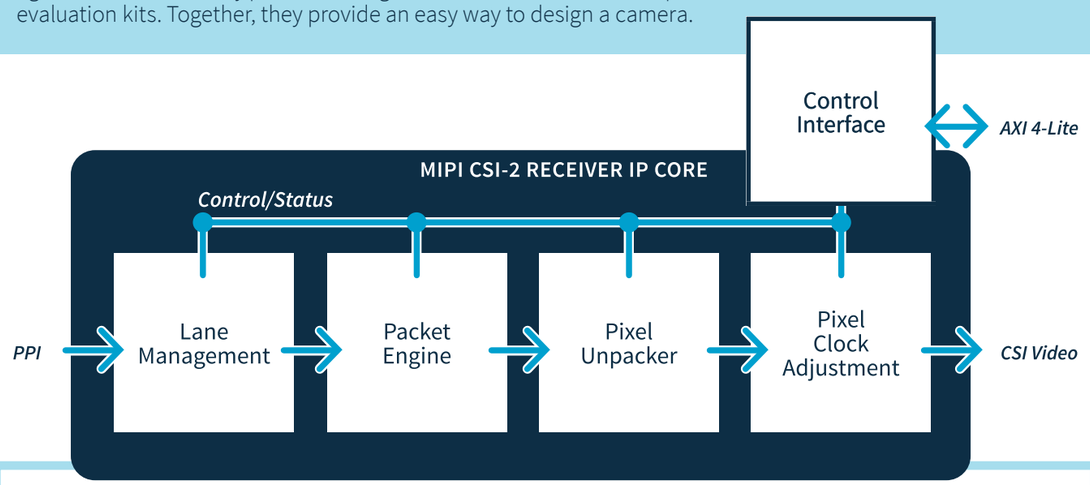


AT A GLANCE

- MIPI CSI-2 receiver and decoding block
- Configurable number of MIPI Lanes
- Using AMD D-PHY IP
- Delivered as working reference design for fast development

MIPI CSI-2 IP Core Description

Image sensors with MIPI interface are not only used in mobile phones, but also in industrial and automotive applications. These applications often require an FPGA for control and further processing. This IP helps to interface MIPI sensors of different vendors to FPGAs. The IP relies on an existing D-PHY implementation, typically available from FPGA vendors. The IP is delivered as a fully functioning reference design that is running on an agreed common delivey platform along with a MIPI FMC module compatible with S2I's MVDK and standard FPGA evaluation kits. Together, they provide an easy way to design a camera.



Main features

- FPGA technology independent
- PPI interface to connect to different D-PHY implementations
- Configurable to 1, 2 or 4 data lanes
- Any lane rate (limited by the used FPGA)
- RAW8, RAW10, RAW12, RAW14, RAW16 standard MIPI data types
- Embedded data decoding
- Direct output of reordered byte stream without pixel unpacking
- AXI4-Lite slave control interface

RESOURCE USAGE

https://www2.euresys.com/S2i-MIPI-CSI-2-IP-Core

MVDK
Machine Vision Development Kit

MVDK Description

S2I's MVDK (Machine Vision Development Kit) is a hardware platform that eases the evaluation and development of products based on S2I's IP Cores and using any major industrial vision interface. The MVDK base board is highly configurable through the use of FMCs (FPGA Mezzanine Cards). It provides an interface to vision sensors and enables the development of GigE Vision, USB3 Vision and CoaXPress cameras (devices), as well as the design of GigE Vision and CoaXPress hosts.

Hardware and Reference Design

The MVDK is delivered with an Enclustra Mercury FPGA module and an FMC interface board. They come along with a fully functioning reference design. Together, they minimize development time and allow for top-notch performance at a small footprint, while leaving enough flexibility to customize the design.

For CoaXPress development

The MVDK delivered for CoaXPress development includes an FMC with two or four CXP-6 or CXP-12 connections for device (camera) or host (frame grabber) design. The device and host reference designs are fully CoaXPress compliant

For USB3 Vision development

The MVDK available for USB3 Vision development is based on the 5-Gbit/s technology of standard USB3 components and allows for the most cost-effective high-speed camera design today. The USB3 Vision IP Core development kit is fully compliant with GenICam and certified by the A3. This is the easiest way to start the design of a new USB3 Vision camera. The USB3 Vision interface is implemented using an FMC designed by S2I that uses a Cypress FX3 USB3 chip

For GigE Vision development

The MVDK delivered for GigE Vision development supports the design of camera and host applications compliant with the A3 GigE Vision specification with a speed of up to 10 Gbps. 2.5, 5 and 10 Gbps applications require an S2I NBase-T FMC module.

For Sony IMX development

S2I's MVDK is compliant with Sony's IMX Pregius series of sensors, a widely used, high-quality CMOS series of imagers. S2I supports these sensors with dedicated IP to read data from and control the sensors. The reference design consists of the IMX IP Core together with a GigE Vision compliant output.

For MIPI CSI-2 development

The MVDK delivered with the MIPI CSI-2 receiver IP Core supports the design of cameras with the widely used, high-quality imagers compliant with MIPI CSI-2 standard. Sensor to Image's IP Core supports reading data from and control the sensors. The reference design consists of the MIPI CSI-2 receiver IP Core together with a GigE Vision compliant output.

Notes

More at www.euresys.com/s2i

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