

## ULL FPGA Framework Hybrid Solution

Harness the combined power of  
FPGA speed and software flexibility



What is the ULL FPGA Framework

### Hardware and software development frameworks

The **ULL FPGA framework** is a high-performance **FPGA and software solution** specifically designed for ultra-low latency networking applications and primarily for high-frequency trading (HFT) applications.

It provides users with the ability to quickly develop a broad portfolio of FPGA applications and gain a competitive edge by processing large amounts of data with near zero latency.

### Accelerate performance and reduce latency

By combining the **high-performance capabilities of FPGA** with the **adaptability of software-based components**, the hybrid Framework delivers low-latency performance while seamlessly integrating into existing systems, scaling effortlessly with growing data, and adapting to evolving market conditions.

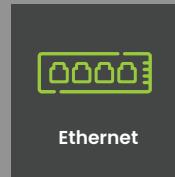
### Get scalability and ongoing support

We support a wide range of hardware and software platforms, so you can **seamlessly integrate our framework** into your existing infrastructure, with scalable solutions that keep pace with the evolution of your business. Our team of experts ensures smooth implementation and ongoing optimization, enabling your trading systems to remain competitive in a dynamic market.

### Typical use cases

- Tick-to-trade electronic trading
- Smart order routers
- Pre-trade risk check engines
- Exchange interconnects

### ULL FPGA FRAMEWORK



Ethernet  
ULL Ethernet MAC/PCS



Network Acceleration  
ULL TCP/IP UDP/IP Offload Engine



PCIe Connectivity  
ULL PCIe DMA Controller

# Solution details

## Complete suite of ULL FPGA IP Cores

All FPGA IP cores achieve extremely low latency performance while maintaining a reasonable timing margin and preserving critical FPGA resources for on-chip computational acceleration.

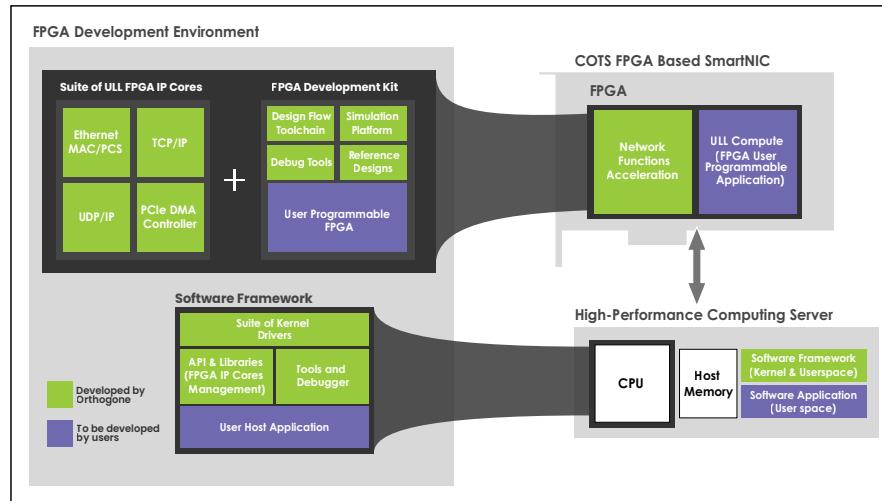
## Development environment and reference design

A comprehensive FPGA development environment including design scripts, end-to-end simulation test benches, a AMD Alveo x3522pv reference design, and a complete suite of Linux drivers, libraries & API, and utility tools are provided to simplify and accelerate project development.

## Flexibility and scalability

With its standard interfaces and highly customizable FPGA cores, the framework can easily support the addition of features and evolve according to your needs while maintaining exceptional performance.

### Orthogone ULL FPGA Framework Solution



## Key Benefits

- Full **RTL implementation** supporting layers 2, 3, 4 (ARP, IPv4, ICMP, TCP, UDP).
- A comprehensive **end-to-end simulation environment**, including a rich library of test cases to streamline validation and verification processes.
- **Highly parameterizable** to meet the specific needs of each application.
- **AMD Alveo™ UL3524, AMD Alveo™ x3522pv, and AMD Alveo™ UL3422 FPGA** platforms reference design examples.
- Complete suite of **Linux drivers, libraries & API**.
- **FPGA timing margins at 644 MHz** for enhanced reliability and performance at the highest clock rates.
- **Tx pre-filled buffers** for instant data readiness and reduced startup latency.
- **Cache warmup** optimization to stabilize PCIe transfers and cut latency jitter.
- **FPGA Hot Reboot enabling reprogramming** without a full server restart.
- Updated toolchain compatibility with **Vivado 2025.1 and XSIM**.
- Expanded OS support with full **Ubuntu integration**.

## FPGA Solutions

### for Ultra-Low Latency SmartNIC

#### Specifications

##### Ultra Low-Latency IP cores:

- **ULL Ethernet MAC & PCS IP Cores**
  - 10G MAC/PCS, RTT **SoP-to-SoF: 17.1 ns** (16b, Sync clocks, 644MHz MAC/PCS)
  - 10G MAC/PCS, RTT **SoP-to-SoP: 34.1 ns** (16b PMA, 32b AXI4-Stream interface, MAC/PCS/CDC)
  - Hardware acceleration for Ethernet packets

##### • **ULL TCP/IP, UDP/IP Offload Engine**

##### **SoP-to-SoP 6.2 ns Tx**

- Hardware acceleration for TCP/IP and UDP/IP protocols
- Now enhanced to run efficiently at 644 MHz for improved throughput and timing

##### • **ULL-PCIE DMA Controller**

Bidirectional data transfer between the host CPU and FPGA through a PCIe interface.

##### **Roundtrip Time:**

**635ns** - Dell/EMC PowerEdge R750 (Intel® Xeon® Gold 5315Y)

**608ns** - Blackcore G3 SPR-M (Intel® Xeon® w7-2495X)

**585ns** - Blackcore ICON 3100-RL+ (Intel® Core™ i9-14900KS)

## Pricing model and support

Several pricing options are available depending on your needs and the platforms you use. We know how to adapt to your project and budget.

Project, site, annualized and card-based licensing options are available.

Contact us today to find the best option for you:

**[sales@orthogone.com](mailto:sales@orthogone.com)**

**T: 1 (514) 316-1917**



Orthogone offers highly specialized engineering solutions focused on the design of innovative products requiring in-depth knowledge of software development, embedded systems and FPGAs.

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