DIGITAL CORE DESIGN

PRESENTATION

IP CORE EXPERT

SINCE 1999

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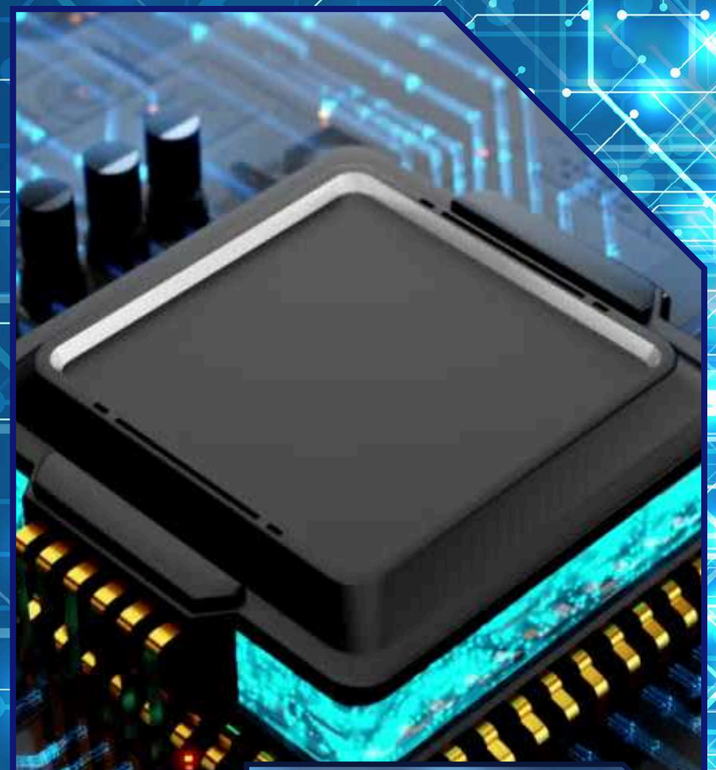

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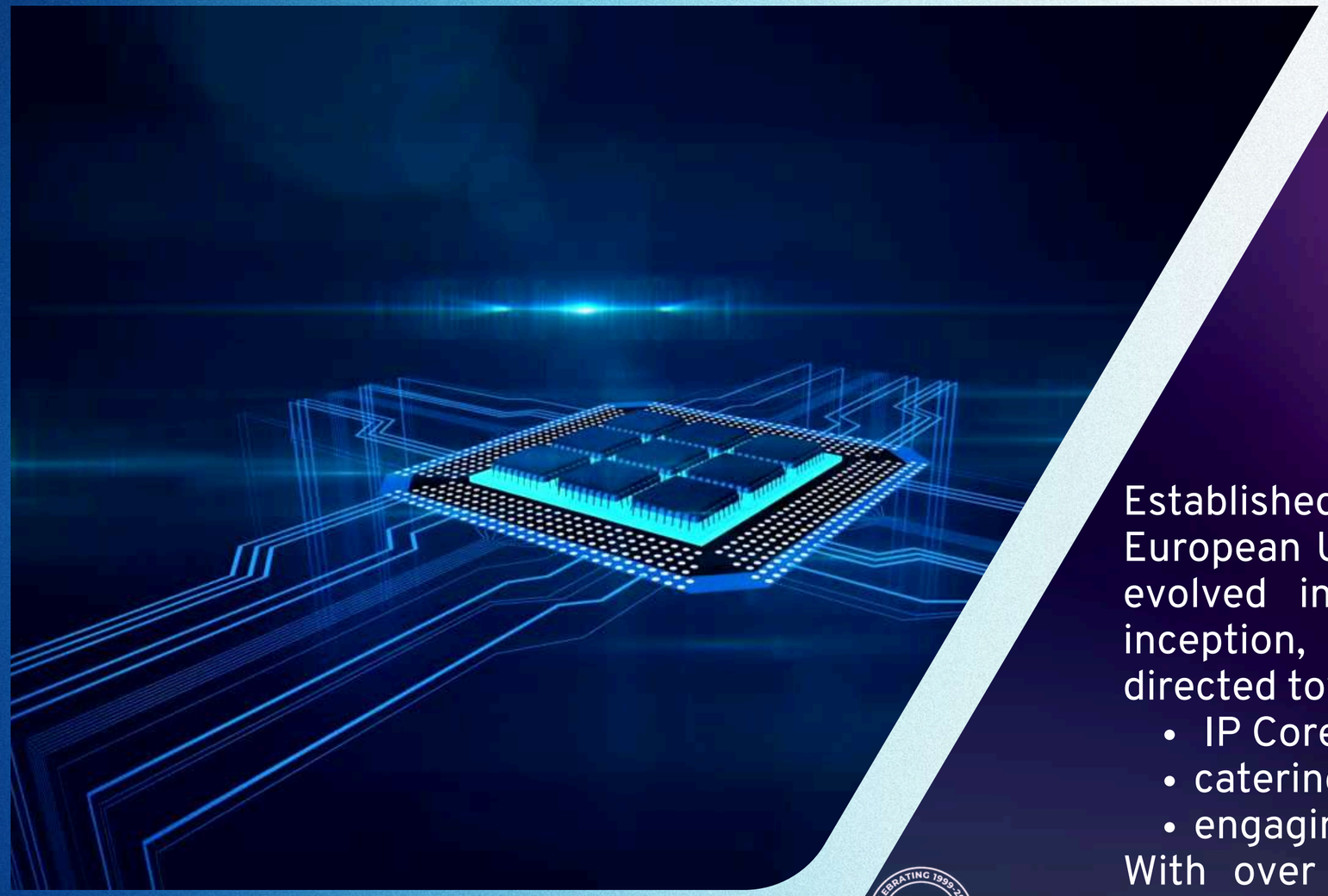
25 YEARS
IN ELECTRONICS

DCD
DIGITAL CORE DESIGN



ABOUT US

Established in 1999 in Bytom, Poland, within the European Union, Digital Core Design (DCD) has evolved into a pioneering force. Since our inception, our focus has been unwaveringly directed towards:

- IP Core & SoC development,
- catering to obsolete parts replacement,
- engaging in R&D ventures.

With over 1 000,000,000 electronic devices worldwide harnessing DCD's solutions and a multitude of satisfied clientele spanning the globe, our impact resonates across industries.

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DCD DIGITAL CORE DESIGN

Digital Core Design has mastered more than 100 different IP Core architectures since 1999; they build holistic ecosystem to simplify your project

Among them you can find e.g. World's Fastest 8051 CPU; Royalty-Free 32-bit CPU; 32-bit & 64-bit RISC-V CPUs; CAN-XL and more

All the IP Cores have been tailored to the customers' needs - most CPUs available with the proprietaty debugger and additional tools

OUR VISION

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Meet Our Team

The DCD team comprises a dynamic blend of seasoned engineers and enthusiastic graduates hailing from top-tier universities. This adept team has honed their skills across over 100 complementary architectures, powering a staggering array of at least 1 billion products.

Jacek Hanke
CEO

Tomek Krzyżak
CTO

Iwill Doit
Engineer

Ino Vation
FAE

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KEY IP CORES

- World’s Fastest 8051/80251 CPU
- World’s Tiniest 8051/80251 CPU
- Royalty-free 32-bit CPU
- 32-bit & 64-bit RISC-V CPUs
- 100% safe cryptographic system
- CAN XL (not only) for automotive
- peripherals and extensions

EDN 2013 HOT 100

European Business Awards

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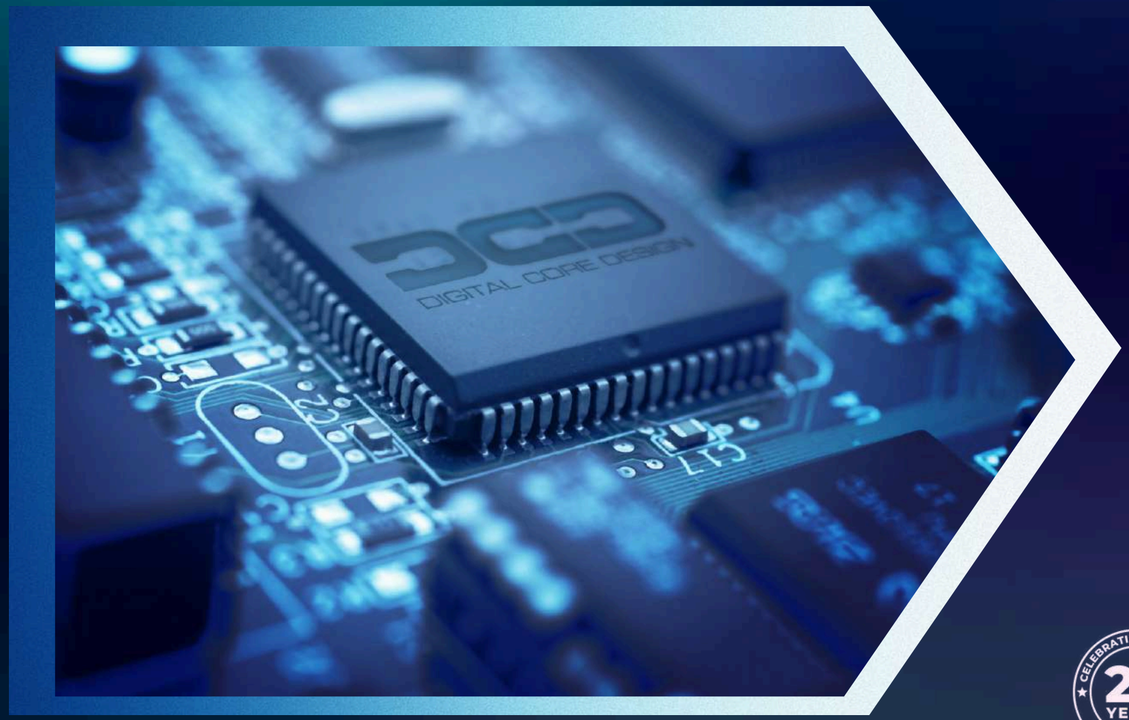
8-BIT WONDER

One of the most popular architecture in the CPU history, Intel’s 8051 has been prepared for 21st centrury - ultimate performance, wide set of peripherals and more for IoT, IIoT, automotive, consumer electronics, embedded.



- DQ80251 is more than 75.times faster than Intel’s original
- just 6k ASIC gates for DT8051
- with DCD’s on chip de-bugger (Debug IP Core +Hardware Assisted De-bugger+Debug Software

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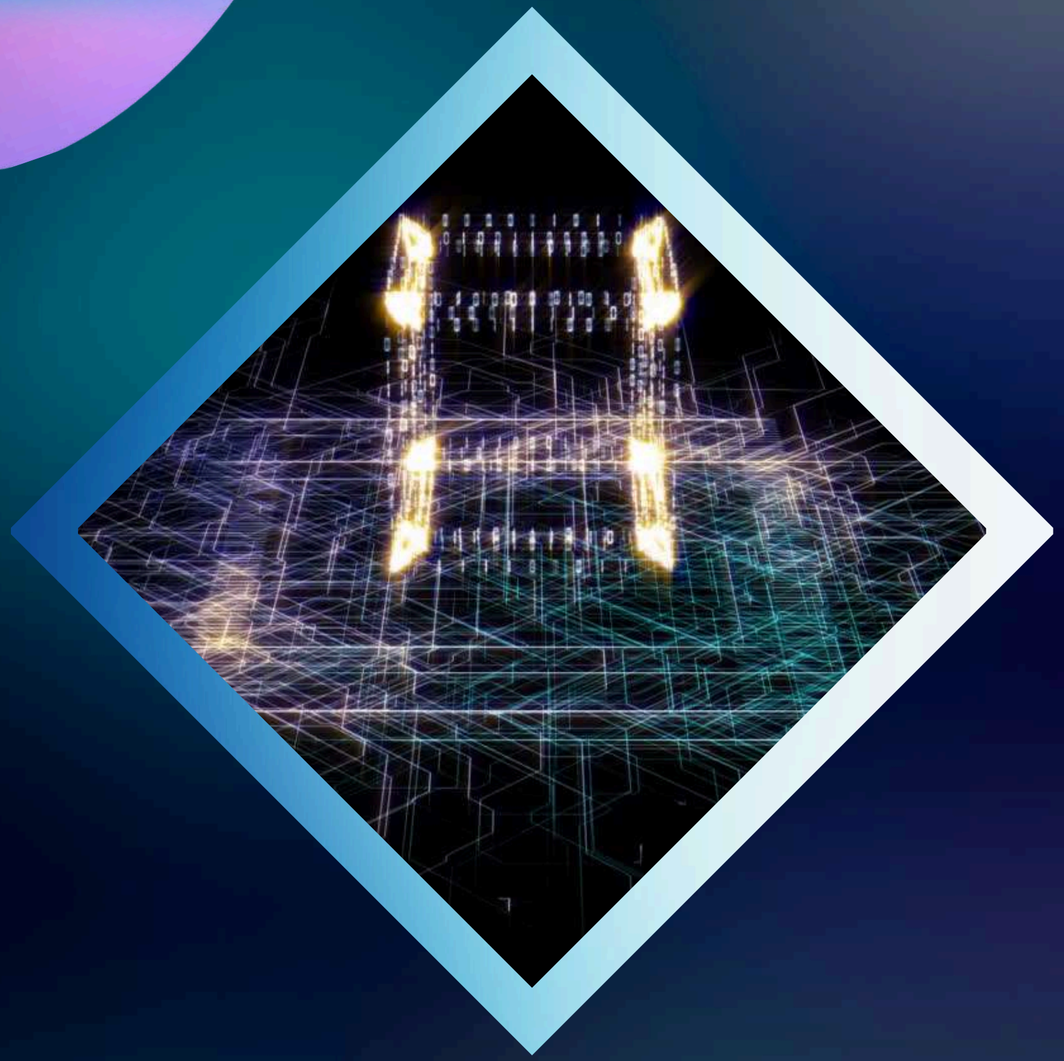

32-BIT RISC CPU

The D32PRO is a royalty-free, silicon proven, high performance soft core of a single-chip 32-bit embedded controller, with Floating Point Coprocessor.

- Configurable 32-bit Harvard architecture
- Performance up to 1.52 / 2.67 DMIPS/MHz and 2.59 CoreMarks/MHz
- Small footprint starting at 10.6k/6.8k ASIC gates
- Very high clock frequency up to 1 GHz in modern ASIC technologies
- Royalty-free

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RISC-V

Digital Core Design is an active member of RISC-V International. RISC-V combines a modular technical approach with an open, royalty-free ISA — meaning that anyone, anywhere can benefit from the IP contributed and produced by RISC-V. As a non-profit, RISC-V does not maintain any commercial interest in products or services. As an open standard, anyone may leverage RISC-V as a building block in their open or proprietary solutions and services.

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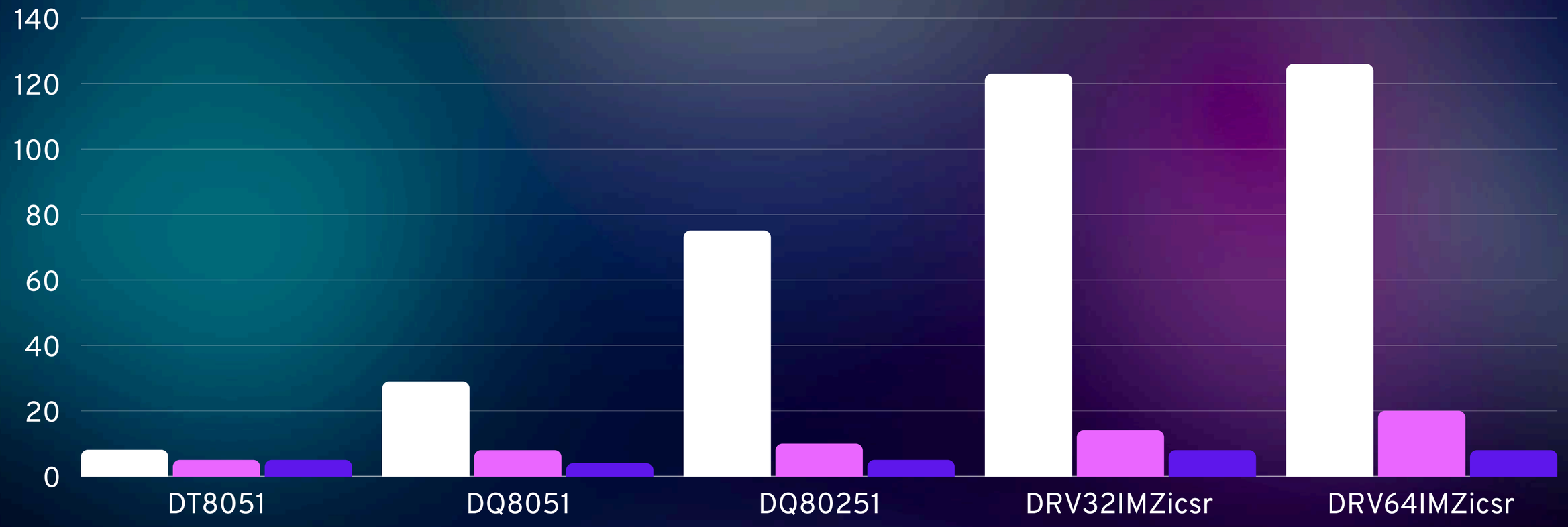
The DRV32IMZicsr is a 32-bit RISC-V CPU with M, Zicsr extensions, and External Debug support:

- a five-stage pipeline,
- Harvard architecture
- flexible size of program and data memory together with their allocation in address space.

Our solution offers performance tailored to the project requirements, starting from:

- Dhrystone: up to 1,23 DMIPS/MHz
- Coremark: up to 2,45 CoreMark/MHz



CPU PERFORMANCE

- Estimated Dhrystone performance for DCD's CPUs. All of them are available with a wide set of peripherals, controllers, ethernet, HDLC, I2C, I2S, I3C, IrDA, Smart Card, SPI, Timers, UART, USB.

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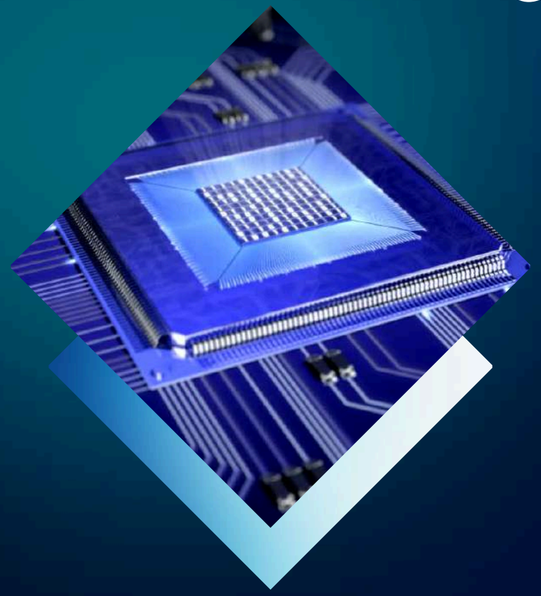
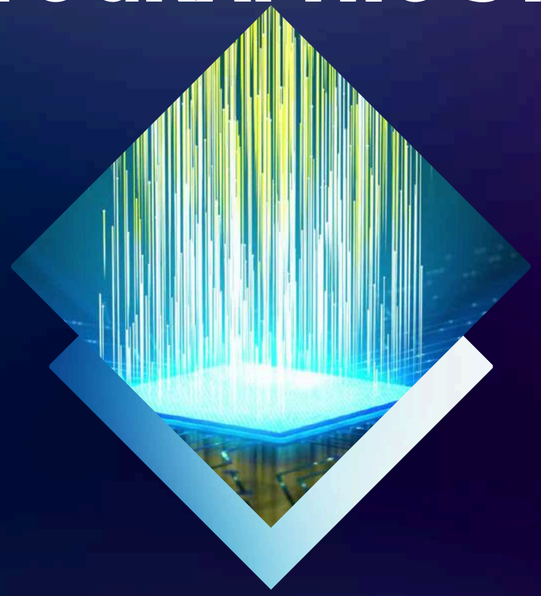
CRYPTONE

CRYPTOGRAPHIC SYSTEM



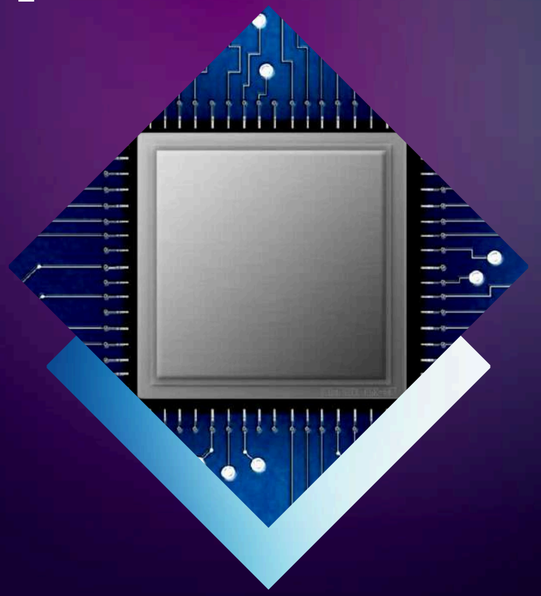
Post-quantum

CryptOne can implement next generation cryptography standards approved by NIST. Thanks to it you can protect your data against future threats with post-quantum hardware encryption.



Hardware crypt

CryptOne – a 100% secure cryptographic system based on more than 20 years of DCD's market experience. It is a universal and fully scalable solution that is able to boost asymmetric cryptographic algorithms.



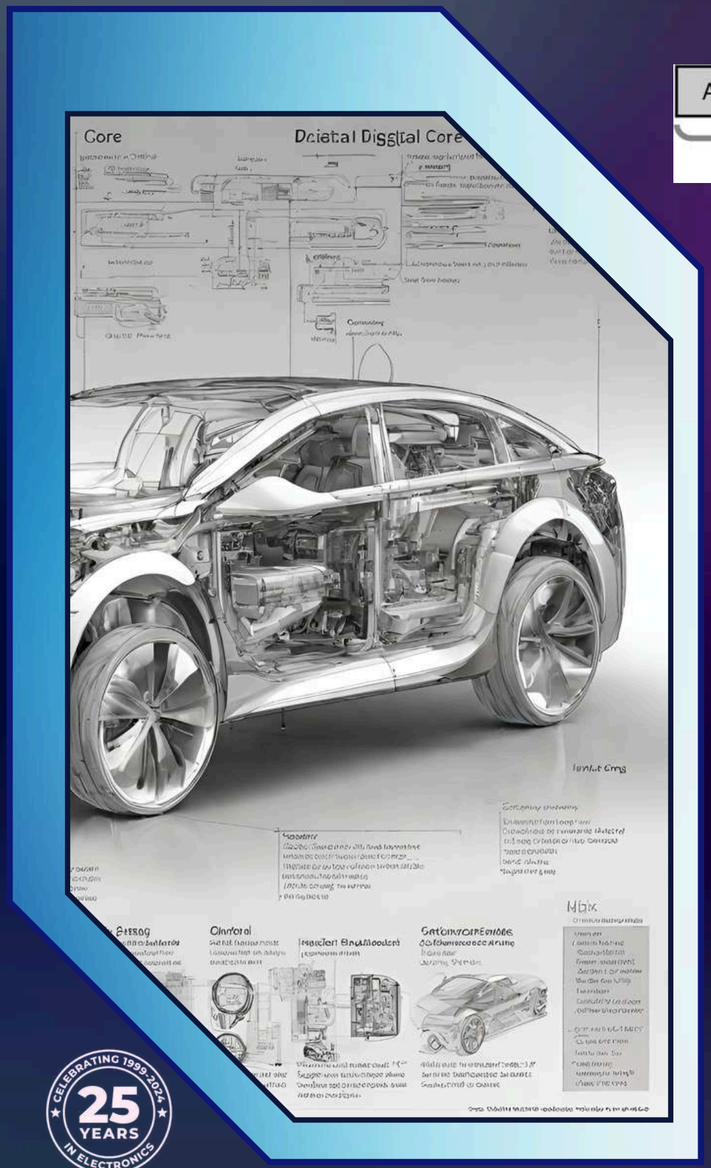
Lightweight crypt

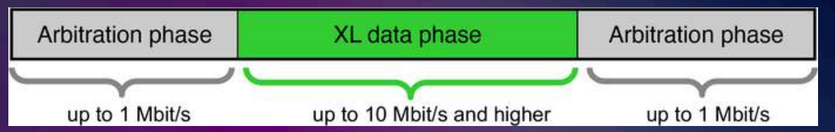
Safety & security meet the best size/performance ratio with: DAES XTS - cryptographic co-processor for lightweight cryptography, ECC verification IP Core, ECDSA signature generation engine, ECDSA verify 384, DSHA2-384 Hash and HMAC Functions Accelerator

CAN-XL

CONTROLLER AREA NETWORK EXTENDED DATA-FIELD LENGTH

CAN-XL represents a paradigm shift, particularly in automotive technology. With speeds reaching up to 20Mbit/s and incorporating Functional Safety measures, this solution seamlessly aligns with the demands of contemporary auto-motive & embedded electronics sectors, among others.
The 3rd generation of the CAN data link layer accommodates all three protocol types (Classical CAN, CAN FD, and CAN XL). Similar to CAN FD, it features two specified bit-timing settings. Notably, the data field length ranges from 1 byte to 2048 bytes.





The IP core comes in two variants: Basic and Safety-Enhanced, following ISO 26262-10 Safety Element out of Context standards.
Documentation encompasses all ISO26262 soft IP SEooC mandated work products, including a thorough Failure Modes Effects and Detection Analysis (FMEDA) with detailed instructions to facilitate IP integration into the customer's system and enable system-level safety analysis.

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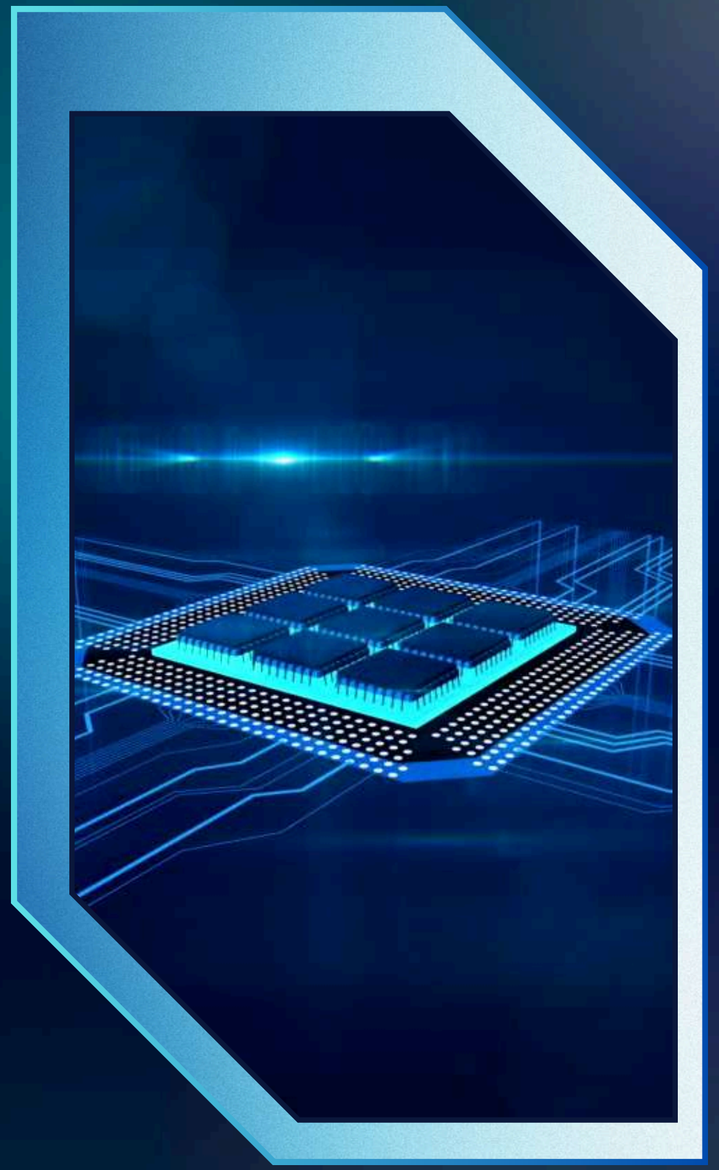

SUMMARY

- 25+ years market experience
- all-in-one from 1 vendor
- holistic portfolio (CPUs+peripherals)
- quality over quantity
- 1 billion products = success stories
- company based in Europe
- close to Intel’s, TSMC’s fabs in Europe

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THANK YOU

DO YOU HAVE ANY QUESTION?

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